Student Training Manual for

CONTROL DATA

CYBER 170 MODEL 720/730

CENTRAL PROCESSOR

VOLUME 2

An Individualized Course

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MODULE 6
SHIFT SEQUENCE

During this module you learn to follow control signals and data paths through the detailed pak diagrams (DPDs) for the logic in the arithmetic section of the CPU associated with shift sequence, which is found on DPD ISC 3.3 in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	6-A	Reference Reading: ISC 3.3 Theory of Operation, Left Shift 20 Instruction. This learning activity covers the left shift 20 instruction.	6-5
_____	_____	6-B	Exercise: ISC 3.3 Theory of Operation Review. This learning activity reinforces what you learned about the left shift 20 instruction.	6-6
_____	_____	6-C	Reference Reading: ISC 3.3 Theory of Operation, Right Shift 21 Instruction. This Learning activity covers the right shift 21 instruction.	6-9

LEARNING ACTIVITY 6-A. REFERENCE READING: ISC 3.3 THEORY OF OPERATION, LEFT SHIFT 20 INSTRUCTION

During this activity you will learn about the control signals and data flow for the 20 instruction, left shift Xi by jk.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data paths for the 20 left shift Xi by jk instruction.

Directions: Locate the following detailed pak diagram (DPD), Theory of Operation description, and the instruction flow Sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the 20 left shift Xi by jk instruction.
- Instruction flow sequence chart for the 20 left shift Xi by jk instruction.

Review the 20 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the 20 instruction while referencing to DPD 3.3 and to the instruction flow sequence chart for the 20 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the 20 left shift Xk by jk instruction, proceed to learning activity 6-B. In learning activity 6-B you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 20 left shift Xk by jk instruction.

LEARNING ACTIVITY 6-B. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW, LEFT SHIFT 20 INSTRUCTION

This activity reinforces what you learned about the 20 left shift Xi by jk instruction in learning activity 6-A.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the 20 left shift Xi by jk instruction.

Directions: The following questions refer to DPD ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 20 left shift Xk by jk instruction. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. Describe the action performed by the 20 left shift instruction. left shift (Xi) by jk

2. What module type and at what location is the module containing the shift sequence timing chain? GW H22

3. On what module type and location is the left shift flip flop located? GW H22

4. On what module and on what detailed pak diagram does the GOSH signal originate? IEC 3.7 (GW)

5. What signal selects the i bits of the instruction as the X register address? SH SLXI

6. On what module and at what location is shift network rank 1 bit 0 located? (UP) B32

7. How many bits feed shift network rank 1? 108

8. On what module at what location is shift network rank 3 bits 0-3 located? UP B32

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 6-B

1. The 20 instruction transfers the contents of the Xi register to the shift network, left shifts it circularly jk positions, and returns it to the Xk register.

2. GW @ H22

3. GW @ H22

4. GU on IEC 3.7

5. SH SLXi

6. UP at B32

7. 108

8. UP @ B33

LEARNING ACTIVITY 6-C. REFERENCE READING: ISC 3.3 THEORY OF OPERATION, RIGHT SHIFT 21 INSTRUCTION

During this activity you will learn about the control signals and data flow for the 21 instruction, right shift Xi by jk.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data paths for the 21 right shift Xi by jk instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the 21 right shift Xi by jk instruction.
- Instruction flow sequence chart for the 21 right shift Xi by jk instruction.

Review the 21 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the 21 instruction while referring to DPD 3.3 and to the instruction flow sequence chart for the 21 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the 21 right shift Xk by jk instruction, proceed to learning activity 6-D. In learning activity 6-D you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 21 right shift Xk by jk instruction.

LEARNING ACTIVITY 6-D. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW RIGHT SHIFT 21 INSTRUCTION

This activity reinforces what you learned about the 21 right shift Xi by jk instruction in learning activity 6-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the 21 right shift Xi by jk instruction.

Direction: The following questions refer to DPD ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 21 right shift Xk by jk instruction. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What action is accomplished by the 21 instruction?
   Right shifts (Xi) by jk

2. What signal enables the exit from the shift sequence to the RNI sequence at T264? ah NEXT

3. What signal causes the jk bits to remain complemented for the right shift? RS

4. On what module and at what location is the SK3, SK4, and SK5 developed? AU UT B24
   AU.3.4

5. On what module and at what location is the SK counter SK 4-6 located? AU 3.4 FS C24

6. On what detailed pak diagram would the RS signal be generated for complement control for the shift count translator UT @ B24? ISC 3.3 GW

7. On what module and at what location is the end case flip flop for the shift sequence located? AU F24

ANSWERS FOR LEARNING ACTIVITY 6-D

1. The 21 instruction is the same as the 20 instruction, except that the shift is right instead of left, lower order bits are shifted off and lost and the vacated higher order bit positions are filled with copies of the exponent sign bit.

2. SHNEXT

3. RS

4. UT @ B24

5. FS @ C24

6. ISC 3.3 on GW module

7. AD @ K22

LEARNING ACTIVITY 6-E. REFERENCE READING: ISC 3.3 THEORY OF OPERATION 22 AND 23 SHIFT INSTRUCTIONS

During this activity you will learn about the control signals and data flow for the 22 and 23 instructions left and right shift Xk (nominally) Bj places to Xi.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data paths for the 22 and 23 left and right shift Xk (nominally) Bj places to Xi instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the 22 and 23 left and right shift Xk (nominally) Bj places to Xi.
- Instruction flow sequence chart for the 22 and 23 left and right shift Xk (nominally) Bj places to Xi.

Review the 22 and 23 instructions, if necessary, in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the 22 and 23 instructions while referring to DPD 3.3 and to the instruction flow sequence chart for the 22 and 23 instructions.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the 22 and 23 left and right shift Xk (nominally) Bj places to Xi instructions, proceed to learning activity 6-F. In learning activity 6-F you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 22 and 23 left and right shift Xk (nominally) by Bj places to Xi.

LEARNING ACTIVITY 6-F. EXERCISE: ISC 3.3 THEORY OF OPERATION 22 AND 23 SHIFT INSTRUCTIONS REVIEW

This activity reinforces what you learned about the 22 and 23 left and right shift Xk (nominally) Bj places to Xi instructions covered in learning activity 6-E.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data paths for the 22 and 23 left and right shift Xk (nominally) Bj places to Xi instructions.

Directions: The following questions refer to DPD ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 22 and 23 left and right shift (nominally) Bj places to Xi intructions. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. Explain the function performed by the 22 instruction. Left shift (Xk) nominally (Bj) places to Xi
2. When the Bj quantity is negative in the 22 instruction, which way is the shift? right
3. Bj is passed to what register during initial common time for the 22 instruction? F
4. What signal is used to indicate that Bj is negative? NBSRJ
5. What does the RS signal accomplish? right shifting
6. What is the maximum shift? What is the maximum shift count? 60 63
7. What bits of U3 are sent to the SK counter via I19 selector at T164 as the Bj portion of the instruction? 0-5
8. What is the routing of Bj to the F register? Bj F3 F2 F
9. What is the routing of Xk to the shift network? Xk I5 C SK
10. Explain the 23 right shift instruction. right shift Xk nominally (Bj) places to Xi

ANSWERS FOR LEARNING ACTIVITY 6-F

1. The 22 instruction transfers the contents of the Xk register to the shift network, shifts it left or right by Bj positions and transfers the result to the Xi register.

2. Right

3. F

4. Nbsrl

5. enables right shifting by its presence

6. 60_{10}; 77_8 or 63_{10}

7. U3 bits 0-5

8. Bj I3 I2 F register

9. Xk I5 Sel C SN

10. The 23 operates in a manner similar to the 22 instruction except that the shift is right if Bj is positive and left if Bj is negative.

LEARNING ACTIVITY 6-G. REFERENCE READING: ISC 3.3 THEORY OF OPERATION, NORMALIZE 24 INSTRUCTION

During this activity you will learn about the control signals and data flow for the normalize 24 instruction, Xk to Xi and Bj.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths used in the execution of the 24 instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the normalize 24 Xk to Xi and Bj instruction.
- Instruction flow sequence chart for shift instructions 24, 25.

Review the 24 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

While reading the theory of operation description for the normalize Xk to Xi and Bj 24 instruction, refer to DPD 3.3 and to the instruction flow sequence chart for the 24 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the normalize Xk to Xi and Bj 24 instruction, proceed to learning activity 6-H. In learning activity 6-H you will be answering questions designed to reinforce your ability to comprehend the logic associated with the 24 normalize Xk to Xi and Bj instruction.

LEARNING ACTIVITY 6-H. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW NORMALIZE 24 INSTRUCTION

This activity reinforces what you learned about the normalize 24 instruction in learning activity 6-G.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths used in the execution of the 24 instruction.

Directions: The following questions refer to DPD ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 24 normalize Xk to Xi and Bj instruction. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers those given at the end of this activity.

1. What function is performed by the 24 instruction?

   normalize (X K) to X i

2. What four processes are normally associated with the (24) instructions? What is a fifth possible process?

   a. Developing normalizing shift count
   b. Shifting coefficient for normalization
   c. Adjusting exponent to compensate for coefficient shift
   d. Packing coefficient and exponent and writing at Xi
   e. [illegible]

3. Explain normalization.

   Shifting the coefficient left until sign bit and bit 47 are not equal and adjusting the exponent [illegible]

4. What happens when an indefinite or infinite operand occurs?

   XK → Xi Bj = 0 [illegible]

5. What signal complements the exponent part of Xk in the I4 selector at T114 if the coefficient is negative?

   S h 1 5 C

6. What happens for an exponent underflow after the shift count is subtracted?

   C o 2 6 4 sets sh and cosigf.

7. What does the RS signal accomplish?

   enable left shifting the coefficient

ANSWERS FOR LEARNING ACTIVITY 6-H

1. The 24 instruction reads a 60-bit floating point operand from Xk, performs a normalize operation on this word, and delivers the normalized result to the Xi register and the normalize count to the Bj register.

2. a. Developing normalizing shift count
   b. Shifting coefficient for normalization
   c. Adjusting exponent to compensate for coefficient shift
   d. Packing coefficient and exponent, storing at Xi
   e. Sequnce exit and halt

3. Normalization involves left shifting the coefficient (bits 0-47) until bit 47 is different from the coefficient sign bit; at this point, the most significant bit of the coefficient is in the highest coefficient position (bit 47). The exponent (bits 48-57) is then decreased by the number of bit positions shifted, to preserve the true size of the word.

4. A shift end case sequence is enabled which sends the Xk operand to Xi unchanged and gates zeros to Bj.

5. Shi5C

6. G0264 sets the end case flip flop to enable sequence exit.

7. The Rs signal enables left-circular shifting by its absence.

LEARNING ACTIVITY 6-I. REFERENCE READING: ISC 3.3 THEORY OF OPERATION, ROUND AND NORMALIZE 25 INSTRUCTION

During this activity you will learn about the control signals and data paths for the round and normalize 25 instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the round and normalize 25 instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the round and normalize 25 instruction.
- Instruction flow sequence chart for the shift instructions 24, 25.

Review the 25 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

While reading the theory of operation description for the round and normalize 25 instruction, refer to DPD 3.3 and to the instruction flow sequence chart for the 25 instructions.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the round and normalize 25 instructions, proceed to learning activity 6-J. In learning activity 6-J you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 25 round and normalize instruction.

LEARNING ACTIVITY 6-J. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW ROUND AND NORMALIZE 25 INSTRUCTION

This activity reinforces what you learned about the round and normalize 25 instruction in learning activity 6-I.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths used in the execution of the round and normalize 25 instruction.

Directions: The following questions refer to the DPD, ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 25 round and normalize instruction.

Answer the following questions by writing the most appropriate word or words in each blan. Compare your answers with thse given at the end of this activity.

1. What function is performed by the (25) instruction?
(Round normally) XR to X is and R1

2. What conditions cause a sequence halt and exits from the 25 instruction? Exponent underflow or overflow on both Plus Minus Zero

3. Explain what happens to bit 107 (the coefficient sign bit) during the 25 instruction. Bit 107 is not interfered with

4. Why does the 25 instruction logic not check for a coefficient equal to zero? BIT 107 will never be zero

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 6-J

1. The 25 instruction operates in a manner similar to the 24 instruction, except that bit 107 (the coefficient sign bit) is set in the C register at T100 before sending C to the shift network. This has the effect of increasing the magnitude of the coefficient by one half the value of the least significant bit position, after the shift is performed.

2. When the operand has an indefinite or infinite exponent or when exponent underflow occurs.

3. Bit 107 ends up in the shifted coefficient right after the previous 2^0 position.

4. The 25 instruction logic does not check for a coefficient equal to zero because the insertion of the round bit makes this condition impossible.

LEARNING ACTIVITY 6-K. REFERENCE READING: ISC 3.3 THEORY OF OPERATION, UNPACK 26 INSTRUCTION

During this activity you will learn about the control signals and data paths for the unpack 26 instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the 26 unpack instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the Instruction Flow Sequence Chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the unpack 26 instruction.
- Instruction flow sequence chart for the shift instruction 26.

Review the 26 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the unpack 26 instruction while referring to DPD 3.3 and to the instruction flow sequence chart for the 26 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the unpack 26 instruction, proceed to learning activity 6-L. In learning activity 6-L you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 26 unpack instruction.

LEARNING ACTIVITY 6-L. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW UNPACK 25 INSTRUCTION

This activity reinforces what you learned about the unpack 26 instruction in learning activity 6-K.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the 26 unpack instruction.

Directions: The following questions refer to the DPD, ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 26 unpack instruction. Answer the questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What operation is performed by the 26 instruction?
unpack Xk to Xi and Bj

2. When does the Xk operand enter the C register via the I5 selector?
Common time

3. What signal enables the exit from the shift sequence to the RNI sequence at T264? SHNEXT

4. What bits of the U3 register define the M position of the shift instruction? 9-11

5. What is the purpose of Shenbc? enables C to receive sign extended coefficient (0 11)

6. Which bit of Xk is considered to be the exponent sign bit?
BIT 66

7. Which bit of Xk is considered to be the coefficient sign bit? Bit 59

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 6-L

1. The 26 instruction reads the operand, unpacks this word from the floating point format, and delivers the coefficient to the Xi register and the exponent to the Bj register.

2. During initial common time

3. Shnext

4. U3 bits 9-11

5. Shenbc enables the C register to receive the coefficient with extended sign bit from the I5 selector at T114.

6. Bit 58

7. Bit 59

LEARNING ACTIVITY 6-M. REFERENCE READING: ISC 3.3 THEORY OF OPERATION PACK 27 INSTRUCTION

During this activity you will learn about the control signals and data flow for the pack 27 instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for 27 pack instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the pack 27 instruction.
- Instruction flow sequence chart for the shift instruction 27.

Review the 27 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

While reading the theory of operation description for the pack 27 instruction, refer to DPD 3.3 and to the instruction flow sequence chart for the 27 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data paths for the pack 27 instructions, proceed to learning activity 6-N. In learning activity 6-N you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 27 pack instruction.

LEARNING ACTIVITY 6-N. EXERCISE: ISC 3.3 THEORY OF OPERATION REVIEW PACK 27 INSTRUCTION

This activity reinforces what you learned about the 27 pack instruction covered in learning activity 6-M.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for the 27 pack instruction.

Directions: The following questions refer to DPD ISC 3.3, the theory of operation description, and the instruction flow sequence chart for the 27 pack instruction. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with the correct answers provided at the end of this activity.

1. What operation is performed by the 27 instruction? Pack Xk and Bj to Xi

2. What is accomplished by the signal Shbi3? _____

3. What is the purpose of Shenbc? enables gating Bj to T3 selector

4. When is the packed word transferred from C to the Xi register? next common word

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 6-N

1. The 27 instruction packs integer quantities from the Xk and Bj registers into the Xi register in floating point format.

2. Shbi3 enables gating Bj into the I3 selector at T114.

3. Shenbc enables clocking the packed word in the I5 selector into the C register at T264.

4. The next common time after the sequence exit.

LEARNING ACTIVITY 6-O. REFERENCE READING: ISC 3.3 THEORY OF OPERATION FORM MASK 43 INSTRUCTION

During this activity you will learn about the control signals and data flow for the form mask 43 instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths for 43 form mask instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.3.
- Theory of operation description for the form mask 43 instruction.
- Instruction flow sequence chart for the shift sequence 43.

Review the 43 instruction, if necessary, in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the form mask 43 instruction while referring to DPD ISC 3.3 and to the instruction flow sequence chart for the 43 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the form mask 43 instructions, proceed to learning activity 6-P. In learning activity 6-P you will be answering questions designed to reinforce you ability to comprehend the logic associated with the 43 form mask instruction.

LEARNING ACTIVITY 6-P. EXERCISE: THEORY OF OPERATION REVIEW FORM MASK 43 INSTRUCTION

This activity reinforces what you learned about the form mask 43 instruction in learning activity 6-O.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths used in the execution of the 43 form mask instruction.

Directions: The following questions refer to DPD ISC 3.3, the theory of operation description and the instruction flow sequence chart for the 43 form mask instruction. Answer the following questions and then check your answers with the correct answers provided at the end of this activity.

1. What operation is performed by the 43 instruction?
form mask (jk) in Xi

2. Where does the jk quantity go and for what purpose?
shift register from a shift count

3. What is the significance of the signal Ffun4?
used to define 43 instruction

4. What is the purpose of the Rs signal in the 43 instruction sequence?
causes a right shift

5. What is the purpose of the Nsh164?
enable JK into the shift count

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 6-P

1. The 43 instruction generates a 60-bit masking word, using the 6-bit jk quantity to designate the width of the masking field.

2. The jk quantity goes to the SK register as a shift count.

3. Ffun4 signal indicates that the f portion of the instruction equals 4.

4. The Rs signal enables transfer of the uncomplemented shift count bits from the shift counter to the shift network.

5. Nsh164 forms a binary count 2 that enables the I9 selector output (jk bits) to enter the SK counter as a preset.

POST TEST

When you have completed the learning activities assigned for module 6, sign on to the PLATO terminal and take the module 6 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 7.

MODULE 7
JUMP SEQUENCES

During this module you learn to follow control signals and data paths through the detailed pak diagrams in the instruction Sequence control (ISC) section of the CYBER 170 CPU Hardware Maintenance Manual for the jump sequence instructions as found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	7-A	Reference Reading: ISC 3.1 Theory of Operation, Normal Jump 02 Instruction. This learning activity covers the normal jump 02 instruction.	7-5
_____	_____	7-B	Exercise: ISC 3.1 Theory of Operation Review, Normal Jump 02 Instruction. This learning activity reinforces what you learned about the normal jump 02 instruction.	7-6

LEARNING ACTIVITY 7-A. REFERENCE READING: ISC 3.1 THEORY OF OPERATION NORMAL JUMP 02 INSTRUCTION

During this activity you will learn about the control signals and data flow associated with the normal jump instruction (02).

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 02 normal jump instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.1
- Theory of operation description for the normal jump instruction
- Instruction flow sequence chart for the normal jump instruction 02

Also locate the normal jump 02 instruction description found in the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review the normal jump 02 instruction description found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the normal jump instruction while referring to DPD ISC 3.1 as well as the instruction flow sequence chart for the normal jump 02 instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the normal jump instruction, proceed to learning activity 7-B. In learning activity 7-B you will be answering questions designed to reinforce your ability to comprehend the logic associated with the normal jump instruction.

LEARNING ACTIVITY 7-B. EXERCISE: ISC 3.1 THEORY OF OPERATION REVIEW NORMAL JUMP 02 INSTRUCTION

This activity reinforces what you learned about the normal jump 02 instruction in learning activity 7-A.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 02 normal jump instruction.

Directions: The following questions refer to DPD ISC 3.1 and the theory of operation description for the normal jump instruction. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. Describe the operation performed by the 02 jump instruction. unconditional jump to K plus zero contents of Bj

2. What signal initiates the normal jump sequence? GONJMP

3. On what module type and at what location is the normal jump timing chain located? Y/B J-28

4. What signal advances the parcel counter during the 02 instruction? NN164

5. What signal enables clocking Bi plus K into the F register at T214? NJFNB/2

6. What signal enables clocking RA from the I3 selector into the E register at T214? NNJX14

7. What is the purpose of Nnjl14 at Tl14? enables clocking BI from I3 selector into E reg. at T114

The answers for this learning activity are on the following page.

ANSWERS TO LEARNING ACTIVITY 7-B

1. The 02 instruction is an unconditional jump to K plus the contents of the Bi register.

2. Gonjmp

3. YB @ J28

4. Nn164

5. Njenbf

6. Nnjx14

7. The Nnjx14 signal enables clocking Bi into the E register from the I3 selector at T114.

LEARNING ACTIVITY 7-C. REFERENCE READING: ISC 3.1 THEORY OF OPERATION BRANCH 030-037 INSTRUCTIONS

During this activity you will learn about the control signals and data flow associated with the conditional jump or branch instructions 030-037.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 030-037 branch instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPD ISC 3.1
- Theory of operation description for the 030-037 branch instructions
- Instruction flow sequence chart for the 030-037 branch instructions

Also locate the description for the 030-037 branch instructions found in the the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review description for the 030-037 branch insructions found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the 030-037 branch instructions while referring to DPD ISC 3.1 as well as the instruction flow sequence chart for the normal jump (branch) instructions 030-037.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 030-037 branch instructions, proceed to learning activity 7-D. In learning activity 7-D you will be answering questions designed to reinforce your ability to comprehend the logic associated with the (030-037) branch instructions.

LEARNING ACTIVITY 7-D. EXERCISE: ISC 3.1 THEORY OF OPERATION REVIEW BRANCH 030-037 INSTRUCTIONS

This activity reinforces what you learned about the 030-037 branch instructions in learning activity 7-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 030-037 branch instructions.

Directions: The following questions refer to DPD ISC 3.1 and the theory of operation description for the 030-037 branch instructions. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given provided at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What is the purpose of the 030-037 instructions? Conditional jump to K depending on the contents of a register
2. What does the signal Coefg0 mean? all 48 bits of the coefficient are zero
3. What signal indicates that the biased exponent in the X register is infinite? NINF
4. What does the signal Zerol indicate? biased exponent in X reg. is zero
5. Which register is used to hold the K? F
6. Which register is used to hold the RA? E
7. Which bits of the U3 register indicate the subgroup 0-7 of the 03X instruction? U3 6-8
8. What does the 030jk perform? Branch to K if X is zero
9. What does the 033jk perform? Branch to K if X is negative
10. What does the Xsrl indicate? X is negative

The answers for this learning activity are on the following page.

ANSWERS TO LEARNING ACTIVITY 7-D

1. The 030-037 instructions are conditional jumps (branches) to K, depending on the result of a jump test.

2. Coefgo is a status signal indicating that all 48 bits of the coefficient in the X register are zero.

3. Ninf1

4. Zero1 is a latched status signal indicating that the biased exponent in the X register is zero.

5. F

6. E

7. U3 bits 6-8

8. Branch to K if (Xj) = 0

9. Branch to K if (Xj) negative

10. Xsr1 is a latched status signal indicating that the value in the X register is negative.

LEARNING ACTIVITY 7-E. REFERENCE READING: ISC 3.1 THEORY OF OPERATION BRANCH 04-07 INSTRUCTIONS

During this activity you will learn about the control signals and data flow associated with the conditional jump or branch instructions 04-07.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 04-07 branch instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.1
- Theory of operation description for the (04-07) branch instructions
- Instruction flow sequence chart for the (04-07) branch instructions

Also locate the description for the 04-07 branch instructions found in the the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review description for the 04-07 branch instructions found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the 04-07 branch instructions while referring to DPD ISC 3.1 as well as the instruction flow sequence chart for the normal jump (branch) instructions 04-07.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the 04-07 branch instructions, proceed to learning activity 7-F. In learning activity 7-F you will be answering questions designed to reinforce your ability to comprehend the logic associated with the 04-07 branch instructions.

LEARNING ACTIVITY 7-F. EXERCISE: ISC 3.1 THEORY OF OPERATION REVIEW BRANCH 04-07 INSTRUCTIONS

This activity reinforces what you learned about the 04-07 branch instructions in learning activity 7-E.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the 04-07 branch instructions.

Directions: The following questions refer to DPD ISC 3.1 and the theory of operation description for the 04-07 branch instructions. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What functions are performed by the 04-07 instructions? Conditional jump to K based on comparison of quantities in Bj and Fm

2. What three processes are required for the execution of the 04-07 instructions? Enabling execution and branch Performing the branch address Jump test

3. What signal sets the RNI initial start FF at T214 if the jump test is met? NJPEXL

4. What signal enables clocking K into the F register via the I2 selector? NNI64

5. What signal enables the sequence exit and starts the next RNI cycle if the jump test is not met? NJMPEX

The answers for this learning activity are on the following page.

ANSWERS TO LEARNING ACTIVITY 7-F

1. The 04-07 instructions are conditional jumps (branches) to K based on the comparison of the quantities in the Bi and Bj registers.

2. a. enabling execution and branch
   b. formation of the branch address
   c. jump test

3. Njpex1

4. Nn164

5. Njmpex

LEARNING ACTIVITY 7-G. REFERENCE READING: ISC 3.0 THEORY OF OPERATION, RETURN JUMP 010 INSTRUCTION

During this activity you will learn about the control signals and data flow associated with the return jump instruction 010.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 010 return jump instruction.

Directions: Locate the following detailed pak diagram DPD, theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPD ISC 3.0
- Theory of operation description for the 010 return jump instructions
- Instruction flow sequence chart for the 010 return jump instructions

Also locate the description for the 010 return jump instructions found in the the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review the description for the 010 return jump instruction found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the 010 return jump instruction while referring to DPD ISC 3.0 as well as the instruction flow sequence chart for the 010 return jump sequence.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 010 return jump instruction, proceed to learning activity 7-H. In learning activity 7-H you will be answering questions designed to reinforce your ability to comprehend the logic associated with the 010 return jump instruction.

LEARNING ACTIVITY 7-H. EXERCISE: ISC 3.0 THEORY OF OPERATION REVIEW RETURN JUMP 010 INSTRUCTION

This activity reinforces what you learned about the 010 return jump instruction in learning activity 7-G.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data path for the 010 return jump instruction.

Directions: The following questions refer to DPD ISC 3.0 and the theory of operation description for the 010 return jump instruction. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given provided at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What operation is performed by the 010 return jump instruction? Stores an unconditional jump instruction to the current program address plus 1 in the word addressed by K-relative address K plus 1 then branches to the relative address K plus 1 plus the contents of KNT occurrence

2. Which detailed pak diagram contains the return jump sequence timing chain? GJ-J 29 ISC 3.0

3. On what module type and at what location is the return jump sequence timing chain located? GJ -J29 ISC 3.0

4. What signal enables the loading of the normal jump code (0400) into bits 54 through 59 of the H register?

5. Which adder is used to add K with RA to form the absolute address for storing the unconditional jump instruction? S0417

6. What signal enables the out-of-range test of K? RTJ214

7. What signal initiates the return jump sequence? GO RTJ

The answers for this learning activity are on the following page.

ANSWERS TO LEARNING ACTIVITY 7-H

1. The 010 instruction stores an unconditional jump instruction (0400) to the current program address plus 1 (P plus 1) in the upper half of relative address K. The program then branches to relative address K plus 1 on the following RNI sequence to begin a subroutine. The last instruction of the subroutine is a branch to K, which returns the program to instruction P plus 1.

2. ISC 3.0

3. GJ @ J29

4. SO4i7

5. F adder

6. Rtj214

7. Gortj

LEARNING ACTIVITY 7-I. REFERENCE READING: ISC 3.0, ISC 3.5 THEORY OF OPERATION, CENTRAL EXCHANGE JUMP 013 INSTRUCTION

During this activity you will learn about the control signals and data flow associated with the central exchange jump instruction (013).

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 013 central exchange jump instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.0, IEC 3.5
- Theory of operation description for the 013 central exchange jump instruction
- Instruction flow sequence chart for the 013 central exchange jump instruction

Also locate the description for the 013 central exchange jump instruction found in the the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review description for the 013 central exchange jump instruction found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the 013 Central Exchange Jump Instruction while referring to DPD ISC 3.0 and IEC 3.5 as well as the instruction flow sequence chart for the exchange jump instructions 013.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 013 central exchange jump instruction, proceed to learning activity 7-J. In learning activity 7-J you will be answering questions designed to reinforce your ability to comprehend the logic associated with the 013 central exchange jump instruction.

LEARNING ACTIVITY 7-J. EXERCISE: ISC 3.0, IEC 3.5 THEORY OF OPERATION REVIEW CENTRAL EXCHANGE JUMP 013 INSTRUCTION

This activity reinforces what you learned about the 013 central exchange jump instruction in learning activity 7-I.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 013 central exchange jump instruction.

Directions: The following questions refer to DPD ISC 3.0, IEC 3.5 and the theory of operation description for the 013 central exchange jump instruction. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What signal is used to initiate the return jump sequence on ISC 3.0 for the 013 central exchange jump? GORTJ

2. Before executing the exchange, what happens to the P register and why? P is set to P+1 so that when exchanged back into program resumes at the next instruction address

3. What does the presence of the signal ncejsw indicate? Setup of CEJ/MEJ switch

4. What signal sets the Illegal FF at Gortj time when 013 code is contained in a parcel other than parcel 0? NSETIL

5. What is the use of Rx14a* at T214? enables E register to receive the contents of B5 from I 3 address

6. What three processes are involved with the execution of the 013 instruction? enabling, execution and exchange formation of CM exchange address incrementing P register

7. Which module type and at what locations are the modules that contain the EXJ timing chain? GF-J25, GF-J24

8. On what module type and at what location is the module that contains the CR9 X FF? GF-J27

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 7-J

1. Gortj

2. It is incremental to P+1; this enables the current program to resume after a return exchange.

3. That the CEJ/MEJ switch on the PPS deadstart panel is enabled.

4. Nsetil

5. Rx14a* at T214 enables clocking of Bj plus K from the F Adder into the F register for formation of the exchange address.

6. a. Enabling execution and exchange
   b. Formation of CM exchange address
   c. incrementing P register

7. GF @ J24; GF @ J25

8. GE @ J27

LEARNING ACTIVITY 7-K. REFERENCE READING: ISC 3.0 THEORY OF OPERATION MONITOR STOP 00 INSTRUCTION

During this activity you will learn about the control signals and data flow associated with the monitor stop or error exit instruction 00.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the (00) error exit and monitor stop instruction.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPD ISC 3.1
- Theory of operation description for the 00 monitor stop or error exit instruction
- Instruction flow sequence chart for the 00 monitor stop or error exit instruction

Also locate the description for the 00 error exit instruction or program stop instruction found in the the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Review the description for the 00 instruction found in the central processor instruction description section of the Hardware Reference Manual. Then read the theory of operation description for the 00 monitor stop instruction while referring to DPD ISC 3.0 as well as the instruction flow sequence chart for the 00 error exit instruction.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 00 instruction, proceed to learning activity 7-L. In learning activity 7-L you will be answering questions designed to reinforce your ability to comprehend the logic associated with the 00 monitor stop or error exit instruction.

LEARNING ACTIVITY 7-L. EXERCISE: ISC 3.0 THEORY OF OPERATION REVIEW MONITOR STOP 00 INSTRUCTION

This activity reinforces what you learned about the 00 monitor stop or error exit instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 00 monitor stop instruction.

Directions: The following questions refer to DPD ISC 3.0 and the theory of operation description for the 00 monitor stop or error exit instruction. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What three processes are involved with the execution of the 00 instruction? [illegible]

2. What signal initiates the return jump sequence timing for the 00 instruction? GORTJ

3. What happens with an 00 instruction when the CEJ/MEJ switch is in the disable position (use table 3)? stops CPU

4. What signal clears the RUNFF at Gortj time if the CEJ/MEJ switch is disabled? NCLRUN

5. What is the purpose of the signal Nr164b? [illegible]

6. What are the uses of the monitor stop instruction? stop CPU [illegible]

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 7-L

1. a. Enabling execution and jump
   b. Formation of the monitor stop instruction
   c. Formation of the RA address

2. Gortj

3. Stops CPU

4. Nclrun

5. The Nr164b signal enables loading the error exit bits into the I7 Selector bits 48 through 53.

6. a. Stops the CPU if error occurs during the execution of another instruction.
   b. An error exit clears the U3 register and forces a decoding of 00.

POST TEST

When you have completed the learning activities assigned for module 7, sign on to the PLATO terminal and take the module 7 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 8.

MODULE 8
FLOATING POINT ADD AND SUBTRACT

During this module you learn to follow control signals and data flow through the detailed pak diagrams for the floating point add/subtract instructions and will include packing and unpacking. The diagrams used in this module include DPD ISC 3.4, ISC 3.5, and ISC 3.6 found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	8-A	Reference Reading: ISC 3.4, 3.5, 3.6 Theory of Operation, General Flow - Floating Point Add/Subtract 30-35 Instructions. This learning activity covers a general flow description of the floating point add/subtract 30-35 instructions.	8-3

LEARNING ACTIVITY 8-A. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION, GENERAL FLOW FLOATING POINT ADD/SUBTRACT 30-35 INSTRUCTION

During this activity you will learn about the control signals and data flow associated with the floating point add/subtract instructions 30-35.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 30-35 floating point add/subtract instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of operation description for the 30-35 floating point add/subtract instructions
- Instruction flow sequence chart for the 30-35 floating point add/subtract instructions

Review the references to floating point arithmetic found in the Programming Information section and references to floating point instruction for add and subtract 30-35 in the CPU instruction section of the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Then read the theory of operation description for the floating point add/subtract 30-35 instructions found in the theory of operation and diagrams manual. When reading the theory of operation refer to DP ISC 3.4, 3.5 and 3.6 as well as the instruction flow sequence charts for the 30-35 instructions.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the floating point add/subtract instructions 30-35, proceed to learning activity 8-B. In learning activity 8-B you will be answering questions designed to reinforce your ability to comprehend the logic associated with the floating point add/subtract instructions.

LEARNING ACTIVITY 8-B. EXERCISE: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION REVIEW, GENERAL FLOW FLOATING POINT ADD/SUBTRACT 30-35 INSTRUCTIONS

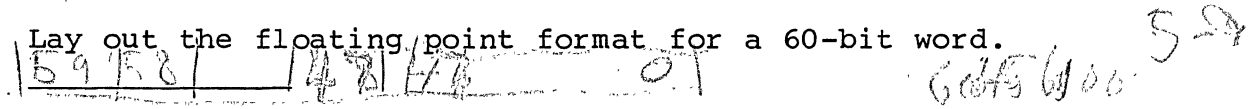
This activity reinforces what you learned about the floating point add/subtract instructions 30-35 in learning activity 8-A.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the 30-35 floating point add/subtract instructions.

Directions: The following questions refer to DPDs ISC 3.4, 3.5 and 3.6 and the theory of operation description for the 30-35 floating point add/subtract instructions. Answer these questions by writing the most appropriate word or words in each blank and compare your answers with those provided at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. Lay out the floating point format for a 60-bit word.

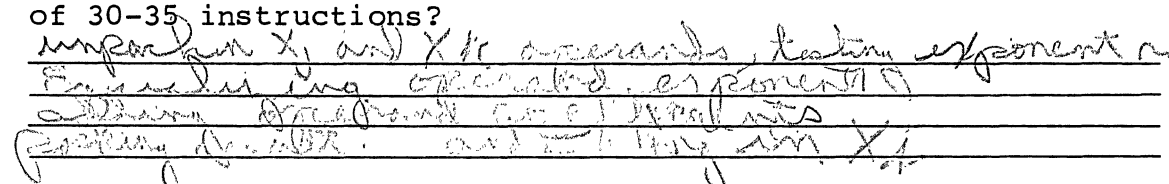


2. What exponent values constitute infinite and indefinite exponents? 3777- 4000) 1777- 6000

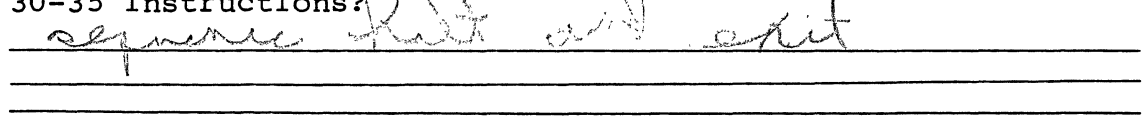
3. The addition or subtraction of floating point numbers requires equal exponents. True or false? True

4. Exponent underflow occurs when the exponent is less than -1777_8 after correction. True of false? True

5. What four processes are normally required for the execution of 30-35 instructions?



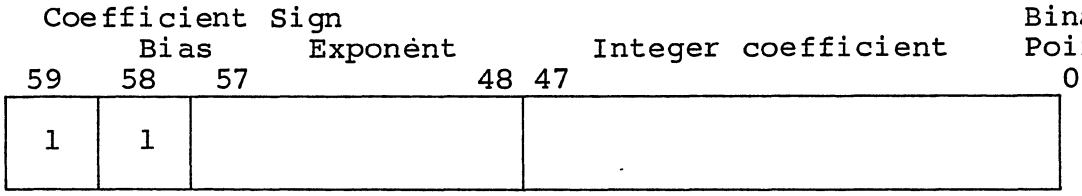
6. What is a fifth possible process required for execution of 30-35 instructions?



The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 8-B

1.



2. infinite $3777_8 + 4000_8$

   indefinite $1777_8 + 6000_8$

3. true

4. true

5. a. unpacking Xj and Xk operands, testing exponent range
   b. equalizing operand exponents
   c. adding operand coefficients
   d. packing result coefficient and exponent, storing at Xi

6. Sequence halt and exit

   a. exponent infinite and indefinite
   b. exponent underflow when adjusted for double precision

LEARNING ACTIVITY 8-C. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION, UNPACKING OPERANDS TESTING RANGE

During this activity you will learn about the control signals and data flow associated with unpacking operands and testing range during floating point add/subtract instructions.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path necessary for unpacking operands and testing exponent range during floating point add and subtract 30-35 instructions.

Directions: Locate the following detailed pak diagrams (DPD's), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of operation description for the 30-35 floating point add/subtract instructions and the specific signals for unpacking operands and testing exponent range
- Instruction flow sequence charts for FAD instructions 30, 31, 32, 33, 34, and 35.

Locate each of the specific signals lsted for: unpacking operands and testing exponent range on the appropriate DPDs. Determine the purpose of each of these signals and be able to describe the purpose of each signal and also describe the data flow expected.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow utilized during the floating point add/subtract instructions for: unpacking operands and testing exponent range, proceed to learning activity 8-D.

LEARNING ACTIVITY 8-D. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION, EXPONENT EQUALIZATION AND COEFFICIENT ADJUSTMENT

During this activity you will learn about the control signals and data flow associated with exponent equalization and coefficient adjustment during floating point add/subtract instructions.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path necessary for exponent equalization and coefficient adjustment during floating point 30-35 add and subtract instructions.

Directions: Locate the following detailed pak diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of operation description for the floating point add/subtract 30-35 instructions and the specific signals for exponent equalization and coefficient adjustment
- Instruction flow sequence charts for FAD instructions 30, 31, 32, 33, 34, and 35.

Locate each of the specific signals lsted for: exponent equalization and coefficient adjustment on the appropriate DPDs. Determine the purpose of each of these signals and be able to describe the purpose of each signal and also describe the data flow expected.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow utilized during the floating point add/subtract instructions for: exponent equalization and coefficient adjustment, proceed to learning activity 8-E.

LEARNING ACTIVITY 8-E. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION PACKING RESULT AND STORING

During this activity you will learn about the control signals and data flow associated with packing result and storing during floating point add/subtract instructions.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path necessary for packing result and storing during floating point add and subtract instructions.

Directions: Locate the following detailed pak diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of operation description for the floating point add/subtract 30-35 instructions and the specific signals for packing result and storing
- Instruction flow sequence charts for FAD instructions 30, 31, 32, 33, 34, and 35.

Locate each of the specific signals listed for: packing result and storing on the appropriate DPDs. Determine the purpose of each of these signals and be able to describe the purpose of each signal and also describe the data flow expected as a result of each signal.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow utilized during the floating point add/subtract instructions for: packing cesult and storing, proceed to learning activity 8-F.

LEARNING ACTIVITY 8-F. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION, SEQUENCE HALT AND EXIT

During this activity you will learn about the control signals and data flow associated with sequence halt and exit during floating point add/subtract instructions.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path necessary for sequence halt and exit during floating point add and subtract 30-35 instructions.

Directions: Locate the following Detailed Pak Diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720,730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of operation description for the floating point add/subtract 30-35 instructions and the specific signals for sequence halt and exit
- Instruction flow sequence charts for FAD Instructions 30, 31, 32, 33, 34, and 35.

Locate each of the specific signals listed for: sequence halt and exit on the appropriate DPDs. Determine the purpose of each of these signals and be able to describe the purpose of each signal and also describe the data flow expected as a result of each signal.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow utilized during the floating point add/subtract instructions for: sequence halt and exit, proceed to learning activity 8-G.

In learning activity 8-G you will be answering questions designed to reinforce your ability to comprehend the logic associated with the specific signals observed in learning activities 8-C, 8-D, 8-E and 8-F.

LEARNING ACTIVITY 8-G. EXERCISE: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION REVIEW SPECIFIC SEQUELS—FLOATING POINT ADD/SUBTRACT

This learning activity reinforces what you learned about specific signals for floating point add/subtract instructions 30-35 in learning activities 8-C, 8-D, 8-E and 8-F.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path necessary for unpacking operands and testing exponent range during floating point add and subtract 30-35 instructions.
- You will be able to locate, identify, and describe the control signals and data path necessary for exponent equalization and coefficient adjustment during floating point 30-35 add and subtract instructions.
- You will be able to locate, identify, and describe the control signals and data path necessary for packing result and storing during floating point add and subtract instructions.
- You will be able to locate, identify, and describe the control signals and data path necessary for sequence halt and exit during floating point add and subtract 30-35 instructions.

Directions: The following questions refer to DPDs ISC 3.4, 3.5 and 3.6 and the theory of operation description for the floating point add/subtract 30-35 instructions and the specific signals for floating point add/subtract 30-35 instructions. Answer these questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity. Reassure yourself of your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. On what detailed pak diagram and on what module type and location is the FAD timing chain located?
   YE-H 25

2. What is the significance of XSR1 and XSR2 on ISC 3.4 (YD)?
   XSR1 X [illegible] XSR2 X [illegible]

3. On what module and at what location are the signals XSR1 and XSR2 generated? YD H 29

4. What signal initiates the floating add sequence by starting the FAD timing chain? G-0 FAD

5. What module type and at what location is the term EXSR2 generated which feeds the UV at J32 on ISC 3.4?
EXP 3.2

6. What is the purpose of the term OddFUN on ISC 3.4 (YD)?
Help determine if X, Y is in Range.

7. What is the significance of the presence of the signal Jltk on ISC 3.4 (YE)? indicates X, Y in multiply

8. What is the purpose of the signal Fadec on ISC 3.5 (HA)? indicate the coefficient or multiplicand

9. What signal indicates that the coefficient sum has overflowed into exponent bit positions 96 through 107? D9LN97

10. Which adder produces the coefficient sum? D

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 8-G

1. DPD ISC 3.4, YE Module @ H25
2. This signal indicates that the coefficient in the X Register is negative.
3. YD @ H23
4. GOFAD
5. GX@F22
6. This signal is used to determine whether Xj or Jk exponent is larger, used in conjunction with Nfeac.
7. This signal indicates the Xj exponent is less than the Xk exponent.
8. This signal indicates the presence of an infinite or indefinite operand.
9. D96 m 97 or ISC 3.6 (GR)
10. D adder

POST TEST

When you have completed the learning activities assigned for module 8, sign on to the PLATO terminal and take the module 8 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 9.

MODULE 9
FLOATING POINT—MULTIPLY AND DIVIDE

During this module you will learn to follow control signals and data flow through the detailed pak diagrams for the floating point multiply and divide instructions. The diagrams used in this module include DPD ISC 3.4, ISC 3.5, and ISC 3.6 found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance manual.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column, put a check mark by each activity assigned to you by PLM. Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	9-A	Reference Reading: ISC 3.4, 3.5, 3.6, Theory of Operation, Floating Point Multiply 40-42 Instructions. This learning activity covers the floating point 40-42 instructions.	9-3
_____	_____	9-B	Exercise: ISC 3.4, 3.5, 3.6, Theory of Operation Review, Floating Point Multiply 40-42 Instructions. This learning activity reinforces what you learned about the floating point multiply 40-42 instructions in learning activity 9-A.	9-4

LEARNING ACTIVITY 9-A. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION FLOATING POINT MULTIPLY 40-42 INSTRUCTIONS

During this activity you will learn about the control signals and data path associated with the floating point multiply instruction 40-42.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 40-42 floating point multiply instructions.

Directions: Review the (40-42) floating point instructions and the floating point arithmetic as described in the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760, Hardware Reference Manual, publication number 60456100.

Locate the following detailed pak diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPDs ISC 3.4, 3.5 and 3.6
- Theory of Operation description for the 40-42 floating point multiply instructions
- Instruction Flow Sequence Chart for FMD instruction 40, 41, and 42

Read the theory of operation description for the 40-42 floating point multiply instructions while referring to DPDs ISC 3.4, 3.5, and 3.6 and the instruction flow sequence chart for the FMD instructions 40, 41, and 42.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data path for the 40-42 floating point multiply instructions, proceed to learning activity 9-B. In learning activity 9-B you will be answering questions designed to reinforce your ability to comprehend the logic associated with the floating point multiply instructions.

LEARNING ACTIVITY 9-B. EXERCISE: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION REVIEW FLOATING POINT MULTIPLY 40-42 INSTRUCTIONS

This activity reinforces what you learned about the floating point multiply 40-42 instructions in learning activity 9-A.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data path for the 40-42 floating point multiply instructions.

Directions: The following questions refer to DPDs ISC 3.4, 3.5, 3.6, to the theory of operation description for the 40-42 floating point instructions, and to the instruction flow sequence chart for the FMD 40, 41, and 42 instructions. Answer these questions and then check your answers with the correct answers provided at the end of this activity. Ensure your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What logical functions are performed by the 40 instruction?
   floating point product of Xj and Xk to Xi
2. What logical function is performed by the 41 instruction?
   Rounded floating point product of Xj and Xk to Xi
3. What logical function is performed by the 42 instruction?
   floating double precision product of Xj and Xk to Xi
4. What tests are made for infinite exponents?
   3777g or 4000g
5. What tests are made for indefinite exponents?
   1777g or 6000g
6. What happens when either Xj and Xk have infinite or indefinite exponents? it results in a sequence fault and enables an error exit on the case exit
7. In processing the 40 instructions, are the exponents made: equal to the smaller; equal to the larger; equal; equal to the sum; equal to the difference of the exponents? _____
   equal to the sum
8. What register holds the partial products during multiplication? Register

9. Which adder is used to form the sum of the exponents? F

10. Identify the four processes that are normally involved with the execution of 40-42 instructions. [illegible]

11. To which register does the Xj coefficient go during initial common time? C

12. To which register does the Xj exponent go during initial common time? F

13. To what value is the shift count translator set at initial common time? 60_8

14. What signal indicates that the shift counter has decremented to zero? SKERO

15. What is the significance of status signals ending in 2, for example, Xsr/2? [illegible]

ANSWERS FOR LEARNING ACTIVITY 9-B

1. The 40 instruction is a floating point product of (Xj) and (Xk) to (Xi).

2. The 41 instruction is a round floating point product of (Xj) and (Xk) to (Xi).

3. The 42 instruction is a floating double-precision product of (Xj) and (Xk) to (Xi).

4. Tests if exponents are 3777_8 or 4000_8.

5. Tests if exponents are 1777_8 or 6000_8.

6. It causes the FMD sequence to halt and enables end case exit.

7. Equal to the sum of the exponents.

8. D register.

9. F adder.

10. a. Unpacking Xj/Xk operands, testing range, alignment of coefficient for multiplication.
    b. Formation and accumulation of partial products
    c. Exponent adjustment and addition.
    d. Parking result and storing.

11. C

12. F

13. 60_8

14. Skeg 0

15. The status signals ending in 2 apply to the second operand (Xk).

LEARNING ACTIVITY 9-C. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION FLOATING POINT DIVIDE 44 and 45 INSTRUCTIONS

During this activity you will learn about the control signals and data path associated with the floating point divide 44 and 45 instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data path for the 44 and 45 floating point divide instructions.

Directions: Review the 44,45 floating point divide instructions as described in the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760, Hardware Reference Manual, publication number 60456100.

Locate the following detailed pak diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPDs ISC 3.4, 3.5, and 3.6
- Theory of operation description for the 44,45 floating point divide instructions
- Instruction flow sequence chart for FMD instruction 44, 45

Read the theory of operation description for the 44,45 floating point divide instructions while refering to DPDs ISC 3.4, 3.5, and 3.6 and to the instruction flow sequence chart for the FMD instructions 44, 45.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data path for the 44,45 floating point divide instructions, proceed to learning activity 9-D. In learning activity 9-D you will be answering questions designed to reinforce your ability to comprehend the logic associated with the floating point divide instructions.

LEARNING ACTIVITY 9-D. EXERCISE: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION REVIEW FLOATING POINT DIVIDE 44 and 45 INSTRUCTIONS

This activity reinforces what you learned about the floating point divide 44,45 instructions in learning activity 9-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the floating point divide 44,45 instructions.

Directions: The following questions refer to DPDs ISC 3.4, 3.5, 3.6, to the theory of operation description for the 44, 45 floating point instructions, and to the instruction flow sequence chart for the FMD 44, 45. Answer these questions and then check your answers with the correct answers provided at the end of this activity. Ensure your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What logically takes place in the 44 instruction? Round Divide XJ by XK to Xm

2. What logically takes place in the 45 instruction? Round Floating Divide and ... similar to XJ by XK to Xm

3. Into what bits of the C register is the division located? 47 to 95

4. Into what bits of the D register is the division located? 47 to 95

5. On what module type and at what location is the module that contains GOFMDC fanout for GO FMD? T2 - G-15

6. On what module type and at what location is the FMD timing chain located? 2N - H24

7. What signal indicates that the biased exponent in the X register is indefinite as shown on the YD module on ISC 3.4? NINDC1/2

8. On what module and at what location is the end case sequence timing chain located? HA G20

The answers to this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 9-D

1. The 44 instruction is a floating point division instruction that divides (Xj) by (Xk) and delivers the result to (Xi).

2. The 45 instruction is a round floating point instruction that divides (Xj) by (Xk) and delivers the result to (Xi).

3. Bits 47 through 95

4. Bits 47 through 95

5. TZ @ G15

6. ZN @ H24

7. Nind1 or Nind2

8. HA @ G20

LEARNING ACTIVITY 9-E. REFERENCE READING: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION POPULATION COUNT 47 INSTRUCTION

During this activity you will learn about the control signals and data path associated with the population count 47 instruction.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 47 population count instruction.

Directions: Review the 47 population count instruction as described in the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760, Hardware Reference Manual, publication number 60456100.

Locate the following detailed pak diagrams (DPDs), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPDs ISC 3.4, 3.5, and 3.6
- Theory of operation description for the 47 population count instruction
- Instruction flow sequence chart for the FMD instruction 47

Read the theory of operation description for the 47 population count instruction while refering to DPDs ISC 3.4, 3.5, and 3.6 and the instruction flow sequence chart for the FMD instruction 47.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data path for the 47 population count instruction, proceed to learning activity 9-F. In learning activity 9-F you will be answering questions designed to reinforce your ability to comprehend the logic associated with the population count instruction.

LEARNING ACTIVITY 9-F. EXERCISE: ISC 3.4, 3.5, 3.6 THEORY OF OPERATION REVIEW POPULATION COUNT 47 INSTRUCTION

This activity reinforces what you learned about the population count 47 instruction in learning activity 9-E.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path for the 47 population count instruction.

DIRECTIONS: The following questions refer to DPDs ISC 3.4, 3.5, 3.6, to the theory of operation description for the 47 population count instruction, and to the instruction flow sequence chart for the FMD 47 instruction. Answer these questions and then check your answers with the correct answers provided at the end of this activity. Ensure your understanding of the material by reviewing the appropriate references for any incorrectly answered questions.

1. What operation is performed by the 47 instruction? Count the number of 1 bits in Xk and [illegible] the count in Xi

2. What two processes are involved with the execution of the 47 instruction? Enter operand into D and [illegible] D reg [illegible] accumulate [illegible] 1 bits counted

3. What flow is required for the counting process in the 47 instruction?

4. What is the value entered into the SK counter during a 47 instruction? 74_8 60_{10}

5. What is the purpose of the signal FENSK?

6. What signal enables the exit from the population count sequence to the RNI sequence? FMDISX

ANSWERS TO LEARNING ACTIVITY 9-F

1. The 47 instruction counts the number of bits in (Xk) and stores the count in (Xi).

2. a. Entry of the operand into the D adder - D register loop and left shifting
   b. Accumulation of 1-bit counts

3. Repeatedly passing the XK operand through the loop consisting of the D adder, the I14 selector, the I4 selector, the D register, and back to the D adder. On each pass through the loop, the I4 selector left shifts the operand one bit position.

4. 74_8 (60_{10})

5. Enables presetting the shift counter to 74_8

6. Fmdex

POST TEST

When you have completed the learning activities assigned for module 9, sign on to the PLATO terminal and take the module 9 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 10.

MODULE 10
COMPARE/MOVE

During this module you will learn to follow control signals and data flow through the detailed pak diagrams for the compare/move instructions. The diagrams used in this module include the Primary block diagrams for the compare move unit (CMU 1.0) and detailed pak diagrams CMU 3.0 through CMU 3.16 found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column below, put a check mark by each activity assigned to you by PLM. Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	10-A	Reference Reading: Compare/ Move Overview. This learning activity provides an overview of the compare/move instructions.	10-5
_____	_____	10-B	Exercise: Compare/Move Overview Review. This learning activity reinforces what you learned about the compare/ move instruction in learning activity 10-A.	10-6

LEARNING ACTIVITY 10-A. REFERENCE READING: COMPARE/MOVE OVERVIEW

During this activity you will be given an overview of the compare/move unit as shown on CMU 1.0 and as it is described in the theory of operation section of the hardware maintenance manual and the instruction description section of the hardware reference manual.

OBJECTIVE

- You will be able to describe the general overview of the compare/move instructions using the primary block diagrams, CMU 1.0, for the compare/move unit, and the theory of operation description.

Directions: Review the description for the compare/move instructions as found in the CYBER 170 Computer Systems Models 720, 730, 740, 750, and 760 Hardware Reference Manual, publication number 60456100.

Locate the primary block diagram for the compare/move unit found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publications number 60456170; also locate the theory of operation description for the compare/move unit (CMU 1.0) found in the hardware maintenance manual.

Read the theory of operation description for the move and compare overview while referencing CMU 1.0.

When you feel comfortable with your understanding of the overview of the compare and move operations proceed to learning activity 10-B. In learning activity 10-B you will be answering questions designed to reinforce your understanding of the compare/move unit overview.

LEARNING ACTIVITY 10-B. EXERCISE: COMPARE/MOVE OVERVIEW REVIEW

This activity reinforces what you learned about the compare/move unit overview in learning activity 10-A.

OBJECTIVE

- You will be able to describe the general overview of the Compare/Move instructions using the Primary Block Diagram, CMU 1-0, for the compare/move unit.

Directions: The following questions refer to the description of the compare/move unit overview. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. On what diagram is the primary block diagram for the compare/move unit located? CMU 1-0
2. What bits of the central memory word refer to character 9? 0-5
3. How many characters may be moved by the move direct (465) instruction? 177₈
4. How many characters may be moved by the move indirect (464) instruction? 17777₈
5. Which registers contain the octal representation of the number of characters to be moved? LA LC
6. Which bits of the instruction word for the move direct (465) instruction specify the: source address? destination address? 30-47 0-17
7. Which registers hold the offset for the K1 address? C1
8. What is the purpose of the offset? ______
9. What is the purpose of LL and LU bits in the designator word for the move indirect (464) instruction? ______

10. How many characters can be compared by the compare collate (466) or the compare uncollate (467) instructions? 177

11. What conditions will cause the compare uncollate (467) instruction to exit? [illegible]

12. Which bits of the instruction word specify the K1 portion of the compare collated (466) instruction? 30-47

13. How is the Xo register set in the compare collated (466) instruction when field K1 is greater than field K2?
0000 0000 0000 0XXX

14. What is the significance of the Ao register in the Compare collated (466) instruction? starting address of collate table

15. What does the upper three bits of the character under examination in the collating table indicate? [illegible]

16. What does the lower three bits of the character under examination in the collating table indicate? [illegible]

ANSWERS FOR LEARNING ACTIVITY 10-B

1. CMU 1.0
2. 0-5
3. up to 127 (177_8)
4. 8191 (17777_8)
5. LA and LC registers
6. 30-47; 0-17
7. C1 for the K1 address
8. It determines which character position in the 60 bit word will start the transfer.
9. The LL and LU bits describe the field length for the move direct (465) instruction.
10. 177_8
11. Compare is completed or two unequal characters are found
12. 30 through 47
13. 0000 0000 0000 0XXX, where XXX is the number of pairs of characters not yet compared in the field plus one
14. Ao register contains the starting word address of an 8-word, 64- character collating table
15. The upper 3 bits are added to the starting address (Ao) to obtain the relative address of the word containing the collated value
16. The lower three bits of the character to be collated specify the character address of the collated value

LEARNING ACTIVITY 10-C. REFERENCE READING: CMU 3.0, 3.1 THEORY OF OPERATION COMPARE/MOVE DATA SECTION

During this activity you will learn about the compare/move data section.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths utilized with the compare/move data section as described in the theory of operation description.

Directions: Locate the compare/move data section part 1 and part 2, description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagrams (DPDs) CMU 3.0 and CMU 3.1 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move data section while referring to CMU 3.0 and CMU 3.1.

When you feel comfortable with your understanding of compare/move data section, part 1 and part 2, proceed to learning activity 10-D. In learning activity 10-D you will be answering questions designed to reinforce your understanding of the compare/move data section.

LEARNING ACTIVITY 10-D. EXERCISE: CMU 3.0, 3.1 THEORY OF OPERATION REVIEW COMPARE/MOVE DATA SECTION

This activity reinforces what you learned about the compare/move data section in learning activity 10-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths utilized with the compare/move data section as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move data section. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. Which register is the 60-bit register that receives C register bits 48 through 107 or R Register bits 0 through 47 and 108 through 113? Q

2. How is the S register used during move instructions 464 and 465? [illegible]

3. Which registers are used to compare data words during compare instructions 466 and 467? Q . S

4. How many characters is each JB pak capable of comparing when doing a S=Q compare? _____

5. During the compare is K1 in the S or Q register? S

6. What signal is generated when all 10 characters in the S and Q registers are equal? CWEQ

7. On what module type and at what location is the S=Q coincident test for character 9 located? JB - C01

8. What logical state will encode bit 3 be if Come bit 2 is a zero? zero

9. Which register stores the first unequal character position code for use later during a collate? CP

10. What is the purpose of the force equivalence bits? _____

11. What register receives the unequal character from S during the compare uncollated instruction? _____

12. What register receives the unequal character from Q during the compare uncollated instruction? 16

13. How many bits does each JD pack compare between TS and TQ? 1

14. What signals are generated from the TS=TQ Coincident Test when the bits 0-5 are equal? CMTC 0

15. On what module and at what locaton is the priority encoder located? JE-D11

16. What is the significance of Rtg bits being logical ones? TQ is greater than TS

17. The Qgs signal from the priority selector is used to condition what register during the exit sequence at the end of the compare instruction? X0

18. During the execution of the compare collate 466 instruction, what is the purpose of the WP register? keep track of D

19. When executing a compare collate 466 and TQ does not equal TS, how is the address of the first collate table address formed? A0 + TS

20. How many CM references are required for collate table look-up when TQ does not equal TS? 2

ANSWERS FOR LEARNING ACTIVITY 10-D

1. Q
2. The S register is a buffer register for data words that have been properly formatted in the Q register. The output of S gates directly to the HR register in instruction execution control.
3. Q and S
4. one
5. S
6. Cweq
7. JB @ C01
8. zero
9. CP
10. The force equivalence bits cause an equal comparison on all characters preceding the unequal character and including the unequal character so the compare collate instruction.
11. TS
12. TQ
13. one
14. Cmtc 0 through Cmtc 5
15. JE @ D11
16. It indicates TQ is greater than TS
17. Ao
18. Keeps track of the last word read from the collate table
19. The contents of Ao are added to TS register bits 3 through 5
20. two

LEARNING ACTIVITY 10-E. REFERENCE READING: CMU 3.2, 3.3 THEORY OF OPERATION COMPARE/MOVE CONTROL SECTION

During this activity you will learn about the compare/move control section.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data paths associated with the compare/move control section as described in the theory of operation description.

Directions: Locate the compare/move control section description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate detailed pak diagrams CMY 3.2 and CMU 3.3 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move control section while referring to CMU 3.2 and CMU 3.3.

When you feel comfortable with your understanding of the compare/move control section, proceed to learning activity 10-F. In learning activity 10-F you will answer questions designed to reinforce your understanding of the compare/move control section.

LEARNING ACTIVITY 10-F. EXERCISE: CMU 3.2, 3.3 THEORY OF OPERATION REVIEW COMPARE/MOVE CONTROL SECTION

This activity reinforces what you learned about the compare/move control section in learning activity 10-E.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths associated with the compare/move control section as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move control section. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. Which register provides the four-bit offset value for the first word of the K2 field? C 1

2. On what module type and at what location is bit 23 of C1 located? _____

3. On what module type and at what location is the C adder located? JX- A12

4. What three functions does the C adder perform?
   add the C 2 and C 1
   subtract C 1 and C 2
   add 1 to C 1 for K field count

5. What is the purpose of Selector I40? _____

6. Name four registers that may be gated by I40 to the Character Select register (CSR)?
   C 1
   C 2
   E 2
   E 3

7. Name three registers that may be gated by I40 to the Partial Write (PW) register?

S < R
L A
L C

8. Name four inputs to LE dependent upon selections made at I40 and I44.

C /
C 2
C 0 /
- 12 9

9. What value representation is entered into LA and LC registers at the beginning of the compare/move instruction?

10. On what module type and at what location is the L adder LADDG2 located?

ANSWERS FOR LEARNING ACTIVITY 10-F

1. C2

2. JX @ A12

3. JY @ B13

4. a. Subtract C2 from C1
   b. Subtract C1 from C2
   c. add 12_8 to shift count

5. I40 Selector provides a four-bit input path to Selector I44 and the I40 Priority Decoder

6. a. C1
   b. C2
   c. LA
   d. LC

7. a. SCR
   b. LA
   c. LC

8. a. C1
   b. C2
   c. complemented contents of the CP register
   d. generated constant of -12_8

9. An octal representation of the character field length

10. JM @ A07

LEARNING ACTIVITY 10-G. REFERENCE READING: CMU 3.4 THEORY OF OPERATION COMPARE/MOVE INSTRUCTION DECODE START SEQUENCE

During this activity you will learn about the compare/move instruction decode start sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move instruction decode start sequence as described in the theory of operation description.

Directions: Locate the compare/move instruction decode start sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also, locate the detailed pak diagram CMU 3.4 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move instruction decode start sequence while referring to CMU 3.4.

When you feel comfortable with your understanding of the compare/move instruction decode start sequence proceed to learning activity 10-H. In learning activity 10-H you will answer questions designed to reinforce your understanding of the compare/move instruction decode start sequence.

LEARNING ACTIVITY 10-H. EXERCISE: CMU 3.4 THEORY OF OPERATION REVIEW COMPARE/MOVE INSTRUCTION DECODE START SEQUENCE

This activity reinforces what you learned about the compare/move instruction decode start sequence in learning activity 10-G.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move instruction decode start sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move instruction decode start sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. What operation is performed by the 460 instruction? Pass

2. What is the signficance of the signal Nilli? Illegal CMU instruction (not in Parcel 0)

3. What signal initiates the instruction decode start sequence? GO CMU

4. What is the signficance of the signal Move? move instruction 464, 465 decoded

5. What sequence signal is generated when the 464 Move indirect is decoded? GIMCS

6. What is the signficance of the Nop signal? a Pass inst. 460 - 463 [illegible]

7. How is the first step for the move 464 and 465 instruction as described in the move instruction description different from the first step for the compare 466 and 467 instruction as described in the compare instruction description?
move [illegible] LR [illegible] LC
Compare [illegible] length in LA are added in [illegible] results returned to LA

The answers to this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 10-H

1. Pass

2. When a CMU instruction is present in any parcel but zero, the illegal instruction signal Nilli is generated.

3. Gocmu

4. The Move signal is present when a move instruction 464, 465 is decoded and absent when a compare instruction 466, 467 is decoded.

5. Eincs

6. A pass instruction 460 through 463 generates a No Operation signal which enables the RNI sequence

7. For the move instruction C2 offset plus, the character length value in LC are added in L adder and returned to LC, whereas in the compare instruction, C1 offset plus character length in LA are added in L adder and returned to LA.

LEARNING ACTIVITY 10-I. REFERENCE READING: CMU 3.5, 3.6, 3.7, 3.8 AND 3.9 THEORY OF OPERATION COMPARE/MOVE ADDRESS SEQUENCE

During this activity you will learn about the compare/move address sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move address sequence as described in the theory of operation description.

Directions: Locate the compare/move address sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed-pak diagrams (DPDs) CMU 3.4, CMU 3.5, CMU 3.6, CMU 3.7, CMU 3.8 and CMU 3.9, found in the hardware maintenance manual.

Read the theory of operation description for the compare/move address sequence while referring to the appropriate detailed pak diagram identified in the description.

When you feel comfortable with your understanding of compare/move address sequence, proceed to learning activity 10-J. In learning activity 10-J you will be answering questions designed to reinforce your understanding of the compare/move address sequence.

LEARNING ACTIVITY 10-J. EXERCISE
CMU 3.5, 3.6, 3.7, 3.8 AND 3.9 THEORY OF OPERATION REVIEW
COMPARE/MOVE ADDRESS SEQUENCE

This activity reinforces what you learned about the compare/move address sequence in learning activity 10-I.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data paths associated with the compare/move address sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move address sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. On what module and at what location is the address sequence timing chain (K114, K164) located? SQ - C20

2. On what module type and at what location is the address sequence timing chain (K214, K264) located? YA C18

3. What condition will the K1 address FF be following the start sequence for a move instruction? reset

4. What condition will the K1 address FF be following the start sequence for a compare instruction? set

5. Is the contents of the K1 or K2 register loaded into the F register during first address for a move instruction 464 and 465? K2

6. Why is the length in LC decremented by 12_8 in the L adder during first address for a move instruction 464 and 465? [illegible]

7. What signal is used to set the K1 address FF at time K264 during first address for a move instruction 464 and 465? SKIALR

8. Is the contents of the K1 or K2 register loaded into the F register during second address for a move instruction 464 and 465? K1

9. What signal indicates an exhaust condition for K1 and sets the K1 exhaust flip-flop during second address? _____

10. When K2 is exhausted during first address the first and last flip-flop is set, the setting of first and last flip-flop enables what sequence? _____

11. What does the buffer counter indicate? _____

12. What is the K1 address FF used for during the second address portion of the move instruction 464 and 465? _____

13. When advancing the K1 address, what signal and what module type and location is the signal generated to enable 1 to F? (Refer to CMU 3.5.) _____

14. What is the purpose of the data counter? _____

15. What is the purpose of Updkpj? _____

16. What is the purpose of Upbkpv? _____

17. During the compare instruction 466 and 467, first address, is K1 or K2 loaded into the F register? _____

18. What is the purpose of the block K address flip-flop during compare instructions? _____

19. What register does the contents of the Ao address register feed during the collate sequence? _____

20. The collate sequence loads the upper bits (3 through 5) of the TQ or TS register into the E register. True or False? _____

ANSWERS FOR LEARNING ACTIVITY 10-J

1. SQ @ C20
2. YK @ C18
3. Reset
4. Set
5. K2
6. This is to test for a K2 exhaust on the first word
7. Sklalr
8. K1
9. Absence of the group carry test (Laddg)
10. One-word sequence
11. The number of K1 words requested from CM, but is decreased by one for every word written into K2.
12. It determines whether the address sequence is to perform additional K1 read requests or formulate the first K2 write address.
13. ltofn; SQ @ C20
14. The data counter contains a count representing the number of words requested from CM.
15. Updkpj increments the data counter by one.
16. Upbkpv increments the buffer counter by one.
17. K1
18. It prevents further address sequences from occurring until the compare sequence compared the first pair of words.
19. F
20. True

LEARNING ACTIVITY 10-K. REFERENCE READING: CMU 3.10, 3.11, 3.12 THEORY OF OPERATION COMPARE/MOVE DATA SEQUENCE

During this activity you will learn about the compare/move data sequence.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data path associated with the compare/move data sequence as described in the theory of operation description.

Directions: Locate the compare/move data sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagrams CMU 3.10, CMU 3.11, and CMU 3.12 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move data sequence while referring to the appropriate detailed pak diagram identified in the description.

When you feel comfortable with your understanding of compare/move data sequence, proceed to learning activity 10-L. In learning activity 10-L you will be answering questions designed to reinforce your understanding of the compare/move data sequence.

LEARNING ACTIVITY 10-L. EXERCISE: CMU 3.10, 3.11, 3.12 THEORY OF OPERATION REVIEW COMPARE/MOVE DATA SEQUENCE

This activity reinforces what you learned about the compare/move data sequence in learning activity 10-K.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move data sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move data sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. What signal starts the data sequence timing chain? CM4CC
2. Name five registers which data from CR9 can move through in succession? H, C, Q, S, HR
3. On what DPD will the Q and S registers be found? CMU 3.0
4. At what time in the data sequence is the realignment of character positions in C performed? D 2 14
5. Is realignment performed by right shifting or left shifting the desired number characters through the shift network and returning the results to C? right
6. What signal is generated during the compare instruction to block D364 to prevent writing? SBARDK
7. The stacking capability provides for the address sequence to monitor the buffer counter to ensure that only (a) fewer K1 address requests (C2 is greater than or equal to C1) or (b) n/a K1 address requests (C1 is greater than C2) can be issued prior to a write.
8. What signal sets the first data FF at the beginning of a CMU instruction? CM4CC

9. When C2 is greater than or equal to C1, which K word is shifted for the Move instruction (464 and 465)? K1

10. What signal forces the Data Counter to be decremented by one? Data ready

11. To which register does the shift residue from the C Register get transferred? R

12. What signal alerts address sequence K264 to initiate a CM Write request? HR full

13. On what module type and at what location is the Data Sequence Timing Chain located? J W [illegible]

14. On what module type and at what location is the Block HR F/F located? H-U-D01

15. What are the three detection flip-flops used in the Data Sequence for the Move Instruction (464 and 465)? [illegible]

16. What condition(s) does the second data path depend during the Second data selection? C2≥C1 a, C1>C2

17. What forces the Data Counter to be decremented by one? Data ready

18. What conditions of First, second and third Data flip-flops exist for the normal path? all clear

19. For what purpose does the Compare instruction (466 and 467) set the Block HR flip-flop? [illegible]

20. During the compare instructions (466 and 467) the selection of the appropriate data path for K1 and K2 is controlled by what F/F? Toggle

21. Is the Toggle F/F set or clear for the selection of K2? set

22. Which of the data selection flip-flops are used during compare instructions? first

23. What prevents loading the C2 offset positions of Q? C2 offset in CSR

24. What is indicated by the condition in the Data Sequence when the Last Compare flip-flop is set and the Buffer count = 2? indicates one remaining pair of words must be transferred and the current buffer is completing

25. What is the accept signal generated by CMC in response to a read or write request? CMCAC

The answers to this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 10-L

ANSWERS FOR LEARNING ACTIVITY 10-L

1. Cmdrjx

2. H; C; Q; S and HR

3. CMU 3.0

4. D214

5. Right Shift

6. Sbhrvk

7. a. five
   b. six

8. Cm4cc

9. K1

10. Data Ready

11. R register

12. HR Full

13. JW @ D08

14. HU @ D09

15. First data; second data; third data

16. C2 greater than or equal to C1; or C1 greater than C2

17. Data Ready

18. First data FF-clear; second data F/F-clear; and third data F/F- clear.

19. Blocks D364 timing signal

20. Toggle FF

21. Set

22. First only

23. The C2 offset in the CSR register.

24. One remaining pair of words must be received and compared before the compare instruction is completed.

25. Cmuocs

LEARNING ACTIVITY 10-M. REFERENCE READING: CMU 3.13 THEORY OF OPERATION COMPARE/MOVE ONE WORD SEQUENCE

During this activity you will learn about the compare/move one word sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move one word sequence as described in the theory of operation description.

Directions: Locate the compare/move data sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagrams CMU 3.13 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move one word sequence while referring to CMU 3.13.

When you feel comfortable with your understanding of compare/move one word sequence, proceed to learning activity 10-N. In learning activity 10-N you will be answering questions designed to reinforce your understanding of the compare/move one word sequence.

LEARNING ACTIVITY 10-N. EXERCISE: CMU 3.13 THEORY OF OPERATION REVIEW COMPARE/MOVE ONE WORD SEQUENCE

This activity reinforces what you learned about the compare/move one word sequence in learning activity 10-M.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move one word sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move one word sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. What condition enables the one word sequence? _____
2. What signal indicates that the last move equals zero? _____
3. During the move instruction, second data, C1 greater than C2, what two things control the loading of Q? _____
4. On what module type and at what location is the shift data sequence timer located? _____
5. What is the significance of the value in the CSR register? _____
6. What is the signficance of the value in the PW register? _____
7. On what module type and at what location is the CSR register located for bits 5, 4, 3, 2? _____
8. For a compare instruction, what is the value in the PW register for a C1 greater than C2 condition? _____

ANSWERS FOR LEARNING ACTIVITY 10-N

1. Enabled when first and sast FF is set, which is during a move when K2 exhausts during first address and for a compare when K1 and k2 exhaust during second address.

2. LmsOTu

3. C2 offset in CSR and the shift count in PW

4. YM @ D16

5. C2 offset is in CSR register.

6. Shift count is in PW register.

7. JZ @ A17

8. Remaining LA value

LEARNING ACTIVITY 10-O. REFERENCE READING: CMU 3.14 THEORY OF OPERATION COMPARE/MOVE COMPARE SEQUENCE

During this activity you will learn about the compare/move compare sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move compare sequence as described in the theory of operation description.

Directions: Locate the compare/move compare sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagram CMU 3.14 found in the hardware maintenance manual.

Read the Theory of Operation description for the compare/move compare sequence while referring to CMU 3.14.

When you feel comfortable with your understanding of compare/move compare sequence, proceed to learning activity 10-P. In learning activity 10-P you will be answering questions designed to reinforce your understanding of the compare/move compare sequence.

LEARNING ACTIVITY 10-P. EXERCISE: CMU 3.14 THEORY OF OPERATION REVIEW COMPARE/MOVE COMPARE SEQUENCE

This activity reinforces what you learned about the compare/move sequence in learning activity 10-O.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move compare sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move compare sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. What two sequences enable the compare sequence? Data

2. What is the significance of Cweg? [illegible]

3. During the Compare Sequence, what is the signficance of the signal Dnboyv? [illegible] Counter by 2

4. What conditions indicate the last compare? K1 exhaust and K2 exhaust on first and last MP slot

5. What signal enables the CP register during compare sequence, comparison unequal condition? EcsRYF

6. Where does the unequal character from S go during the compare sequence, comparison unequal condition? T S

7. What instruction determines that the compare sequence enables the collate sequence? 466

8. What is the purpose of Eexnyf during the compare sequence, comparison equal? [illegible] equal to collate sequence

The answers to this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 10-P

1. Data sequence and collate sequence

2. Cweg is present for an equal compare
   Cweg is absent for an unequal compare

3. Dnboyv decrements the buffer counter by two, so the address sequence will initiate read requests for another pair of words.

4. K1 exhaust and K2 exhaust or first and last FF set.

5. Ecsryf

6. TS

7. 466

8. When the last comparison is an equal condition Eexnyf enables the exit sequence.

LEARNING ACTIVITY 10-Q. REFERENCE READING: CMU 3.15 THEORY OF OPERATION COMPARE/MOVE COLLATE SEQUENCE

During this activity you will learn about the compare/move collate sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move collate sequence as described in the theory of operation description.

Directions: Locate the compare/move collate sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagram CMY 3.15 found in the hardware maintenance manual.

Read the theory of operation description for the compare/move collate sequence while referring to CMU 3.15.

When you feel comfortable with your understanding of the compare/move collate sequence proceed to learning activity 10-R. In learning activity 10-R you will be answering questions designed to reinforce your understanding of the compare/move collate sequence.

LEARNING ACTIVITY 10-R. EXERCISE: CMU 3.15 THEORY OF OPERATION REVIEW COMPARE/MOVE COLLATE SEQUENCE

This activity reinforces what you learned about the compare/move collate sequence in learning activity 10-Q.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move collate sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move collate sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. On what detailed pak diagram is the compare/move collate sequence located? H2-D13 CMU 3.15

2. On what module type and at what location is the collate sequence timing chain located? H2-D13 [illegible]

3. What signal enables the collate sequence timing chain? CM4.CC

4. Which of the collate sequence timing signals are considered part of collate I? Which are part of collate II? CS 114
   1 CS 164 CS 214
   2 CS 264

5. What condition is indicated by the address 2 F/F? indicates [illegible]

6. What does the require address FF allow? [illegible]

7. Which bits of TS or TQ select the the of eight possible collate table words? 3, 5

8. What signal indicates that both collate characters are equal? CC EQ

9. On what module type and at what location and on what DPD is the TQ = TS comparison made? _____

10. On what module type and at what location is the TQ register for bit 5 located? _____

ANSWERS FOR LEARNING ACTIVITY 10-R

1. CMU 3.15

2. HZ @ D13

3. $\overline{\text{CWEQ}}$

4. Collate I - CS114, CS164, CS214
   Collate II - CS264

5. Indicates that two passes through the address sequence must be performed, since both collate characters are located in different words.

6. The require address flip-flop allows the address sequence to be enabled by enabling CS214.

7. Upper three bits (3 through 5)

8. CCEQ

9. JE @ D11 on CMU 3.1

10. JD @ B22

LEARNING ACTIVITY 10-S. REFERENCE READING: CMU 3.16 THEORY OF OPERATION COMPARE/MOVE EXIT SEQUENCE

During this activity you will learn about the compare/move exit sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move exit sequence as described in the theory of operation description.

Directions: Locate the compare/move exit sequence description in the theory of operation section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. Also locate the detailed pak diagram CMY 3.16 found in the hardware maintenance Manual.

Read the theory of operation description for the compare/move exit sequence while referring to CMU 3.16.

When you feel comfortable with your understanding of the compare/move exit sequence proceed to learning activity 10-T. In learning activity 10-T you will be answering questions designed to reinforce your understanding of the compare/move exit sequence.

LEARNING ACTIVITY 10-T. EXERCISE: CMU 3.16 THEORY OF OPERATION REVIEW COMPARE/MOVE EXIT SEQUENCE

This activity reinforces what you learned about the compare/move exit sequence in learning activity 10-S.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data path associated with the compare/move exit sequence as described in the theory of operation description.

Directions: The following questions refer to the description of the compare/move exit sequence. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. On what module type and at what location is the exit sequence timer flip-flops located? YF-D 19

2. What is the enable exit signal generated when K1 and K2 are exhausted during a move instruction? EFXNVF

3. Two timing chain sequence steps are not used in the Move instruction exit sequence, which are they? T 1 T 14

4. What is the compare move unit exit signal that enables the RNI sequence? EB XNVF

5. Name two conditions that will generate enable exits during a compare instruction?

6. What difference exists for exits from the compare collate instruction compared to compare instructions?

7. What register is used to contain the remaining count after an unequal compare? LAC 2

The answers to this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 10-T

1. YF @ D19

2. Eexnvf

3. E164 and E214

4. Ncmuex

5. a. Unequal compare before last compare
   b. Last compare is equal

6. Exit when an unequal compare occurs after the appropriate collate characters are read and compared.

7. LAC 2

POST TEST

When you have completed the learning activities assigned for module 10, sign on to the PLATO terminal and take the module 10 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 11.

4358B

MODULE 11
CPU DIAGNOSTICS

During this module you will become familiar with various diagnostic programs used in the normal maintenance testing of the CYBER 170 CPU. You will learn the basic testing concepts used in the various diagnostics. You will become familiar with the keyboard commands and the associated running and error displays.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column, put a check mark by each activity assigned to you by PLM. Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

Assigned	Completed	Activity	Description	Page
_____	_____	11-A	Reference Reading: CT1 Description. This learning activity covers the diagnostic CT1.	11-5
_____	_____	11-B	Exercise: CT1 Description Review. This learning activity reinforces what you learned about the diagnostic CT1 in learning activity 11-A.	11-13
_____	_____	11-C	Reference Reading: EJ1 Description. This learning activity covers the diagnostic EJ1.	11-15

CYBER 170 Model 720/730 CPU
Module 11

LEARNING ACTIVITY 11-A. REFERENCE READING: CT1 DESCRIPTION

During this activity you will learn about the diagnostic CT1.

OBJECTIVE

- You will be able to describe the purpose of CT1; describe the parameters required to execute CT1; and describe the results expected (normal and abnormal) from the execution of the diagnostic CT1.

Directions: Read the CT1 Description included in the next few pages of this learning activity.

Then locate the fixed operand command test (CT1/CTC) description found in volume 2 of the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, publication number 60160600. Familiarize yourself with the information on pages CT1-1 through CT1-42.

When you feel comfortable with your understanding of CT1 proceed to learning activity 11-B. In learning activity 11-B you will be answering questions designed to reinforce your ability to comprehend the descriptions and use of CT1.

CYBER 170 Model 720/730 CPU
Learning Activity 11-A

CT1 DESCRIPTION

CT1 is a fixed operand command test which was originally written for the 6XXX mainframe and then modified to keep current with each new series (CYBER 70 and 17X). CT1 is a standalone test which is divided into two parts. The first part, called CQL, is a quick look test which is run to determine four things: 1) verify a portion of Central Memory 2) perform an exchange jump test 3) verify the A, B, and X registers and 4) check those instructions which are needed to properly execute part 2 of CT1. If part 1 executes correctly, part 2, called CTC, is loaded and executed. CTC is a comprehensive test of all the CPU instructions excluding compare move.

CT1 consists of the following four routines:

1. CT1 - Monitor and control program for CTC - resides in PPU 1

2. CTC - Comprehensive CPU command test (part 2) - resides in CM between locations $1\text{-}50000_8$

3 CQL - Monitor and quick look programs - resides in PPU0

4 1CQ - Overlay for CQL - resides in CM between locations $60000 - 61600_8$

When CT1 is called from SMM the following sequence is performed (refer to figure 11-1).

1. SMM loader program loads CT1 into PPU1

2. SMM loader program loads 1CQ into CM starting at 60000_8

3. SMM loader program loads CTC into CM starting at 000001_8

4. SMM loader program loads CQL into PPU0

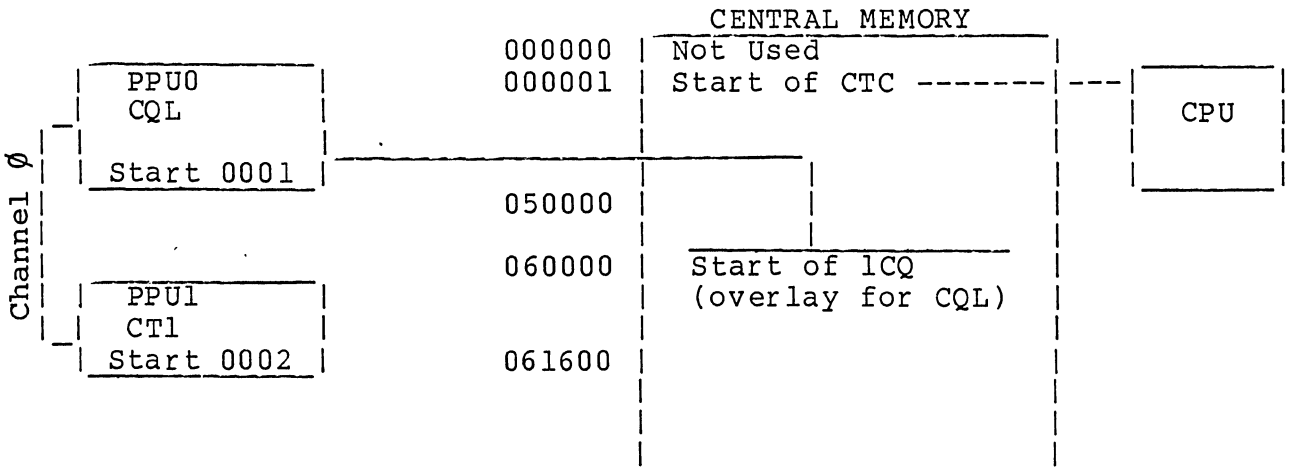


Figure 11-1. CT1 CONFIGURATION

Once loaded, the programs in both PPUs are started. However, the CT1 program in PPU1 is stopped after it initializes a few CM locations. It must then wait for CQL (quick look) to finish in PPU0. CQL signals CT1 to resume execution by activating Channel 0. CT1 will then start executing part two of the test (CTC), which is the comprehensive check of all CPU instructions.

The following is a list of the instructions in the order in which they occur within CT1. By referencing the attached chart, figure 11-2, it should be possible to isolate the area of the machine not previously used, and then through the block diagrams, the possible failing pak(s).

Section I - Quick Look

1. Exchange Jump with all 0s — See EJT for possible failing
2. Exchange Jump with all 1s — hardware components

3. Boolean, 10 instruction
4. Boolean, 14 instruction
5. Increment, 72 instruction - Check X path thru F adder
6. Increment, 62 instruction - Check B as a result register
7. Increment, 61 instruction - Check B as a source register
8. Increment, 51 instruction - Check A as a result register
9. Increment, 50 instruction - Check A as a source register
10. Increment, 52 instruction - Check central read capability
11. Increment, 71 instruction - Check X central read result register

12. Boolean, 11 instruction - Checks logical product (X5-X4)
13. Boolean, 13 instruction - Checks logical difference (X4-X3)
14. Branch, 02 instruction - Checks basic 02 jump
15. Branch, 030 instruction - Checks jump on X = 0
16. Branch, 06 instruction - Jump on B register compares
17. Branch, 04 instruction - Jump on B register compares
18. Branch, 01 instruction - Check return jump.

This ends the quick-look of the test. The previously successfully executed instructions ensure that part 2 of the test can successfully execute in the CPU. In part 2 the instructions are fully checked out as opposed to the partial checks made in the quick-look section.

19. Boolean, 10 inst. -
20. Boolean, 14 inst. -
21. Boolean, 12 inst. -
22. Boolean, 16 inst. -
23. Boolean, 11 inst. -
24. Boolean, 15 inst. -
25. Boolean, 13 inst. -
26. Boolean, 17 inst. -
27. Increment, 70 inst. -
28. Increment, 71 inst. -
29. Increment, 60 inst. -
30. Increment, 50 inst. -
31. Increment, 61 inst. -
32. Increment, 51 inst. -
33. Increment, 62 inst. -
34. Increment, 72 inst. - These increment instructions all use the sum of 2 registers.
35. Increment, 52 inst. -
36. Increment, 63 inst. -
37. Increment, 73 inst. -
38. Increment, 53 inst. -
39. Increment, 64 inst. -
40. Increment, 74 inst. -
41. Increment, 54 inst. -
42. Increment, 66 inst. -
43. Increment, 76 inst. -
44. Increment, 56 inst. -
45. Increment, 65 inst. -
46. Increment, 75 inst. - These increment instructions all involve the difference of 2 registers.
47. Increment, 55 inst. -
48. Increment, 67 inst. -
49. Increment, 77 inst. -
50. Increment, 57 inst. -

51. Long Add, 36 inst. -
52. Long Add, 37 inst. -
53. Branch, 03X inst. - X=0-7
54. Branch, 04 inst. -
55. Branch, 05 inst. -
56. Branch, 06 inst. -
57. Branch, 07 inst. -
58. Shift, 20 inst. -
59. Shift, 21 inst. -
60. Shift, 43 inst. -
61. Shift, 22 inst. -
62. Shift, 23 inst. -
63. Shift, 27 inst. -
64. Shift, 26 inst. -
65. Shift, 24 inst. -
66. Shift, 25 inst. -
67. Floating Add, 30 inst. -
68. Floating Add, 32 inst. -
69. Floating Add, 31 inst. -
70. Floating Add, 33 inst. -
71. Floating Add, 34 inst. -
72. Floating Add, 35 inst. -
73. Floating Mult., 42 inst. -
74. Floating Mult., 40 inst. -
75. Floating Mult., 41 inst. -
76. Floating Divide, 44 inst. -
77. Floating Divice, 45 inst. -

CYBER 170 Model 720/730 CPU
Learning Activity 11-A

How To Use

1. General flow of use
   a. Deadstart
   b. Load CT1 CT1 (CR)
   c. Enter parameter changes
   d. Start test space bar
   e. Quick look section will execute
   f. Quick look error - see attached chart (figure 11-2).
   g. No error - Part 2 takes control
   h. Start (space bar)
   i. Part 2 executes
   j. Part 2 error - Refer to attached chart.
   k. No error - Return to H or deadstart

2. Error isolations procedure
   a. Observe error display and note failing instruction
      1) Quick Look (Part 1) - XXX Test
         XXX = Instruction type
      2) Part 2 - IITXSY
         II = Instruction type
         X = Test number
         Y = Section number
         For example: 24T1S2
         24 inst., test 1, Section 2
   b. Consult test sequence list (under description) and list instruction types executed prior to the failing instruction.
   c. Consult instruction type-hardware used cross reference chart. List, in order of occurrence, inst. type and hardware used.
   d. Note any register, inverter group, control function, and so forth used for the first time by the failing instruction.
   e. Note from display, failing bits (if possible).
   f. Using failing bit(s) and failing hardware component, consult CPU DPD diagrams and swap possible failing pak.
   g. Example - 36T2S3

      OP = 1432 1657 1560 2715 1732
      OP2 = 1111 1111 1111 1111 1111
      CR = 2543 2770 2671 4026 3043
      TR = 2543 2770 2671 4025 3043

      1) Failing inst. = 36
      2) Failing bit = 212
      3) Previously used inst. = exchange 10-17, 50-77
      4) Hardware not previously used: Add functions on D ALU
      5) Possible pak - FD at H05

CYBER 173 CPU INSTRUCTION TO HARDWARE CROSS REFERENCE CHART

INST.	D	DALU	114	ITER-SHIFT 14	115	15	15 COMP	C	SN	H/L SEL	NN	19	SK	119	10	13	13 COMP	12	E	F	FALU	RANGE TEST	FOR EXP TEST	X	B	A	CNST GEN. −139	INST.	DESCRIPTION
00															X	X	N	X	X	X	ADD							00	PROG. STOP
010															X	X	N	X	X	X	ADD	X						010	RETURN JP
013																X	N	X	X	X	ADD							013	C.E.J.
02															X	X	N	X	X	X	ADD	X						02	UNCOND. JP
030-037															X	X	N	X	X	X	ADD	X						030-037	Xi JP
04-07															X	X	Y&N	X	X	X	ADD	X						04-07	B_j JP
10						48-107	Y	48-107		U														X_i				10	XMIT
11	48-107	A&C·D	X	NS		48-107	Y	48-107		U														X_i				11	LOGICAL PROD.
12	48-107	A&C~D	X	NS		48-107	Y	48-107		U														X_i				12	LOGICAL SUM
13	48-107	A&C (~) D	X	NS		48-107	Y	48-107		U														X_i				13	LOGICAL DIFF.
14						48-107	N	48-107		U														X_i				14	XMIT COMP.
15	48-107	A&C·D	X	NS		48-107	N	48-107		U														X_i				15	LOG. PROD. COM.
16	48-107	A&C~D	X	NS		48-107	N	48-107		U														X_i				16	LOG. SUM. COM.
17	48-107	A&C (~) D	X	NS		48-107	N	48-107		U														X_i				17	LOG. DIFF. COM.
20						48-107	Y	48-107	LS 48-107	U		X	X	X										X_i				20	LEFT SHIFT
21						48-107	Y	48-107	RS ALL	U		X	X	X										X_i				21	RIGHT SHIFT
22-23						48-107	N	48-107	LS~RS	U		X	X							X		F	X_i				22-23	SHIFT NOM.
24-25					X	48-107	Y&N	48-107	LS	U	X	X	X			X	Y&N	X	X	X	ADD		F&EXP.	X_i	B_j			24-25	NORMALIZE
26					96-107	48-107	Y OR N	48-107		U						X	Y OR N	X		X				X_i	B_j			26	UNPACK
27					X	48-107	N	48-107		U						X	Y OR N	X		X				X_i				27	PACK
30-35	00-107	A&C THRU	X	NS,RS	X 96-107	00-107	Y&N	00-107	RS	U OR L		X	X			X	Y&N	X	X	X	ADD OR SUBT		F&EXP.	X_i			60_8	30-35	FLT. PT. SUM. DIFF.
36	48-107	ADD	X	NS		48-107	Y&N	48-107		U														X_i				36	INTEGER SUM.
37	48-107	ADD	X	NS		48-107	N	48-107		U														X_i				37	INTEGER DIFF.
40-42	00-107	A&C THRU	X	RS,LS, NS	X	00-107	Y&N	00-107	RS	U OR L			X			X	Y&N	X	X	X	ADD&F		F&EXP.	X_i			60_8~01_8	40-42	FLT. PT. MULT.
44-45	00-107	A&C THRU	X	RS,LS	X	00-107	Y&N	00-107		L			X			X	Y&N	X	X	X	ADD&F		F&EXP.	X_i			60_8~01_8	45-45	FLT. PT. DIV.
43						48-107	N	48-107	RS	U		X	X	X										X_i				43	MASK
47	48-107	C THRU	X	LS	X	48-107	Y&N	48-107		U		X	X			X	N	X	X	X	ADD			X_i			01_8	47	POP. COUNT
50-57															X	X	Y&N	X	X	X	ADD	X				A_i		50-57	INCR. A
60-67																X	Y OR N	X	X	X	ADD				B_i			60-67	INCR. B
70-77					X	48-107	Y OR N	48-107		U						X	Y OR N	X	X	X	ADD			X_i				70-77	INCR. X
COMMON TIME	D=0			14 = 0	48-65	48-107	Y	48-107				19 = 60_8	SK = 60_8		X	X		X	X	X								

Figure 11-2. Cross Reference Chart

LEARNING ACTIVITY 11-B. EXERCISE: CT1 DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic CT1 in learning activity 11-A.

OBJECTIVE

- You will be able to describe the purpose of CT1; describe the parameters required to execute CT1; and describe the results expected (normal and abnormal) from the execution of the diagnostics CT1.

Directions: The following questions refer to the description and use of the diagnostic CT1. Answer these questions and then check your answers with the correct answer provided at the end of this activity.

1. What is the purpose of the CT1 diagnostic program? _____

2. What is the purpose of CT1 part 1 and from where does it execute? _____

3. Which keyboard command is used to start CT1 running? _____

4. What command could be used to clear the CT1 "Stop on Error" flag? CSE

5. Where does the program referred to CTC reside? CTC _____

ANSWERS FOR LEARNING ACTIVITY 11-B

1. CT1 is used to test the CPU instruction set. It checks all CPU instructions except the compare move instructions.

2. CT1 part 1 is a quick look test which executes in PPU0. Its purpose is to verify enough of the CPU hardware is functional to get part 2 of the test running.

3. SPACE BAR

4. CSE

5. CTC resides in CM from address 000001 through address 50000_8.

LEARNING ACTIVITY 11-C. REFERENCE READING: EJ1 DESCRIPTION

During this activity you will learn about the diagnostic EJ1.

OBJECTIVE

- You will be able to describe the purpose of EJ1; describe the parameters required to execute EJ1; and describe the results expected (normal and abnormal) from the execution of the diagnostic EJ1.

Directions: Read the EJ1 description included in the next few pages of this learning activity, 11-C, in this student manual.

Also, locate the exchange jump test (EJT) description found in volume 2 of the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, volume 2, publication number 601606000. This section will provide a description for EJT which is similar for EJ1, although EJ1 is a modification of EJT for CYBER 170s. Become familiar with the information on pages EJT-1 through EJT-12.

Locate the EJ1 description found in the 6000/CYBER 70/CYBER 170 SMM Supplement Manual, publication number 60409500. Become familiar with the EJ1 description.

When you feel comfortable with your understanding of EJ1, proceed to learning activity 11-D. In learning activity 11-D you will be answering questions designed to reinforce your ability to comprehend the description and use of EJ1 and EJT.

CYBER 170 Model 720/730 CPU
Learning Activity 11-C

EJ1 DESCRIPTION

EJ1 is the CYBER 17X exchange jump test. Its purpose is to test the CP exchange jump circuits using the PP EXN instruction 260, the diagnostic checks exchange jump timing, the data paths, and also the P & RA adder (small adder). The test uses all PPUs and channels 1, 11, 12, and 16_8. All CM is used. PPU0 executes the main test body and also handles keyboard input and display functions. PP1 communicates with PPU0 on channel 1. PPU1 is used in section 1 to exchange the CPU and it is used in section 6 to write to central memory. PP11_8 uses channel 11_8 to communicate with PPU0. PP11_8 is used in section 6 to read central memory. The remaining PPUs, $2\text{-}10_8$, are used in each section as conflict PPs. That is, they each loop on a central memory one word read instruction (f=60). Channel 12 is used to transfer the loop routine to each of the conflict PP's. EJ1 uses many of the standard parameter entries and it also has a few unequal ones. The test can be speeded up by using the "T" command, which turns off the memory portion of the display.

LEARNING ACTIVITY 11-D. EXERCISE: EJ1 DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic EJ1 in learning activity 11-C.

OBJECTIVE

- You will be able to describe the purpose of EJ1; describe the parameters required to execute EJ1; and describe the results expected (normal and abnormal) from the execution of the diagnostic EJ1.

Directions: The following questions refer to the description and use of the diagnostic EJ1. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. How many PPUs are needed to execute the EJ1 diagnostic?

2. What is the purpose of section 3 in the EJ1 diagnostic?

3. What is the keyboard command that could be used to clear the EJ1 "STOP ON ERROR" parameter?

4. How can the EJ1 execution time be speeded up?

5. What command could be used to force EJ1 to execute section 1 only?

6. What type of CPU instruction is used in section 2 of EJ1 to check the P+RA adder (small adder)?

7. The EJ1 diagnostic is failing with the error message "PP-1 HUNG." Which PPU instruction has probably failed to execute properly?

8. An EJ1 failure in section 1 would most likely indicate a data rather than a control related problem. True or False? False

9. Which portion of central memory is used by the EJ1 diagnostic? CM

10. EJ1 has failed with the error message "CENTRAL P INCORRECT EXP P= 001000 GOT P=001001". Which section of EJ1 has most likely failed? section 1

The answers to this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 11-D

1. Three PPUs; 0, 1, and 9

2. Section 3 is a data path test. It uses a "worst" pattern to check the various data paths used during an exchange jump operation.

3. CSE (CR)

4. Depressing the T key on the keyboard

5. 0077 X 0001 (CR). This command would set bit 0 in word 77 which selects section 1 only.

6. 71 instruction is used in section 2.

7. The most likely failing instruction would be the EXN (F=260) instruction.

8. False

9. All of CM is used.

10. This a section 1 error message.

LEARNING ACTIVITY 11-E. REFERENCE READING: CT3 DESCRIPTION

During this activity you will learn about the diagnostic CT3.

A microfiche viewer will be required for portions of this activity.

OBJECTIVE

- You will be able to describe the purpose of CT3; describe the parameters required to execute CT3; and describe the results expected (normal and abnormal) from the execution of the diagnostic CT3.

Directions: Read the CT3 description inlcluded in the next few pages of this learning activity, 11-E, in this student manual. The microfiche titled CT3 Diagnostic Program Listings will be utilized in this description.

Also locate the random instruction test with simulation (CT3) description found in the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, Volume 2, publication number 60160600. Become familiar with the information on pages CT3-1 through CT3-14.

When you feel comfortable with your understanding of CT3 proceed to learning activity 11-F. In learning activity 11-F you will be answering questions designed to reinforce your ability to comprehend the description and use of CT3.

INTRODUCTION TO CT3

Although CT3 may be used to test functional units of the CPU, its primary purpose is to check the control portion of it. Because of the large number of possible combinations of registers, instructions, functional units, and operands, this hardware is best tested using random numbers. These random numbers are used in the formation of instruction sequences (loops) and operands to be used by these instructions. Given a known seed (starting number), the random number generator will produce random numbers which will always be in the same sequence. This is useful as a particular failing loop can always be repeated.

Once the random instructions and operands are generated, the resulting set of instructions are executed twice, once by the CPU and once by an instruction simulator. These two results are compared, and depending upon the setting of some parameters, these results (if a failure is detected) are displayed, stored, or printed, and the test halts or may continue.

CT3 has many parameters available for controlling its execution. These are all explained in the documentation for the test. Many of these will be explained later, in the usage section of this course.

USING CT3

The purpose of this section is to alert you to any pitfalls of the test and give any pointers that may be helful in using it.

1. Because CT3 uses a CPU simulator, the possibility exists that the simulator produces an incorrect result. This possibility is quite remote, but keep it in mind.

2. If CT3 is run for an equal amount of time whenever it is used, the same series of random numbers is always executed. By changing the random number generator seed (address 2) an entire new series of numbers is generated.

3. When one functional unit is failing intermittently, you can use the parameters at addresses 12 through 46 to define only instructions which use the failing unit. This will tend to produce an error in less time than normal running would.

4. Using these same parameters (addresses 12 through 46) you are able to eliminate all instructions which use the failing unit. This may be useful in determining if additional units are also producing failures.

5. When it is desirable to allow CT3 to run for a long period of time without close monitoring by a CE, set the parameter in address 5=0. This will result in the error being dumped and execution continuing. This is also handy in recording any intermittent failures.

6. When a given pass count is known to fail, use the parameter in address 7 to get to the failing loop in a hurry. This is also useful if, in the course of working on a problem, the failing loop is destroyed or otherwise lost.

7. Note the memory locations of the machine answers, simulator answers, pass count, and so forth. In the case of an intermittent, by loopon without stopping and observing these locations, a toggling bit or bits sometimes can be seen.

8. The locations of machine answers, simulator answers, pass count, and so forth, may not agree with those in the manual. Use caution when troubleshooting.

CT3 Documentation

At this time locate the microfiche titled "CT3 Diag. Prgm Listings", and insert it in the viewer. Position the viewer at grid location B1 which should correspond to page 1 of the listing. Find the beginning of the documentation section of the listing (usually within the first four pages). Review the documentation paying particular attention to basic philosophy, parameters, commands, and display information.* Gain an understanding of the general concepts before looking at detailed flowcharts and section descriptions. Try to determine general flow of the test including testing sequence, PPUs and channel used, central memory usage and PPU/CPU residence.

NOTE

When you are through studying the CT3 documentation on the microfiche, return to this activity and continue reading at the next topic, CT3 Displays.

CT3 Displays

We will now look at some actual CT3 displays. These displays were made from photographs taken of a CYBER 170 display console. The purpose of these displays is to familiarize you with the actual running/error displays for the diagnostic. Your success

* If you are not familiar with the general organization of a Compass listing, refer to pages 11-57 and 11-58.

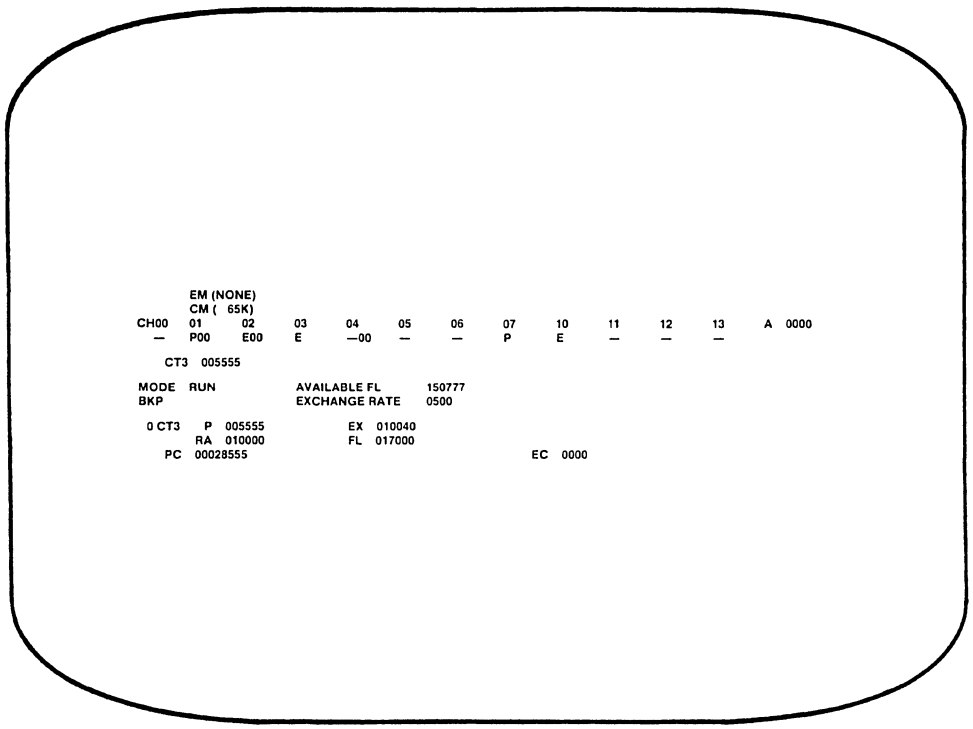
or failure in using CT3 effectively will depend largely on whether or not you can correctly interpret the information presented on these displays.

Reference #1 - CT3 Running Display

Since CT3 normally runs under control of EXC, its running display is the same as CMS or any other diagnostic running under EXC. Note that both the P register and the pass count are changing, which is the normal indication of a running test.

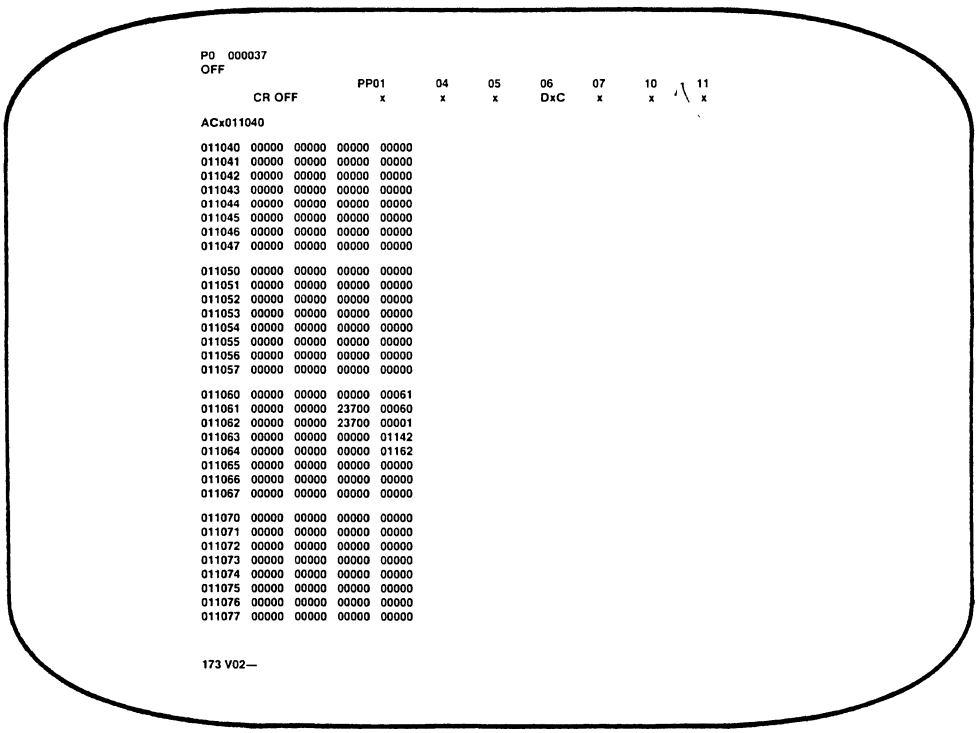
Reference #2 and #3 - CT3 Failure

Test CT3 does not generate an error display when an error is detected. Picture 2 shows central memory when CT3 has detected an error. Address 11060=register difference, 11061=the simulator result, 11062=machine result. Addresses 11063 and 11064 point to the address of the simulator and machine results respectively. These point to picture 3. Picture 3 contains the simulator andmachine results in exchange package format. Since Address 11140 represents (P), (A0), (B0), Address 11142 (RA 10000+1142) represents (FL), (A2), and (B2). With this information we can determine that the error is an incorrect result in register B2. Comparing (11142 and 11162[machine result]) confirms this conclusion. This same information is contained in address 11061 and 11062.



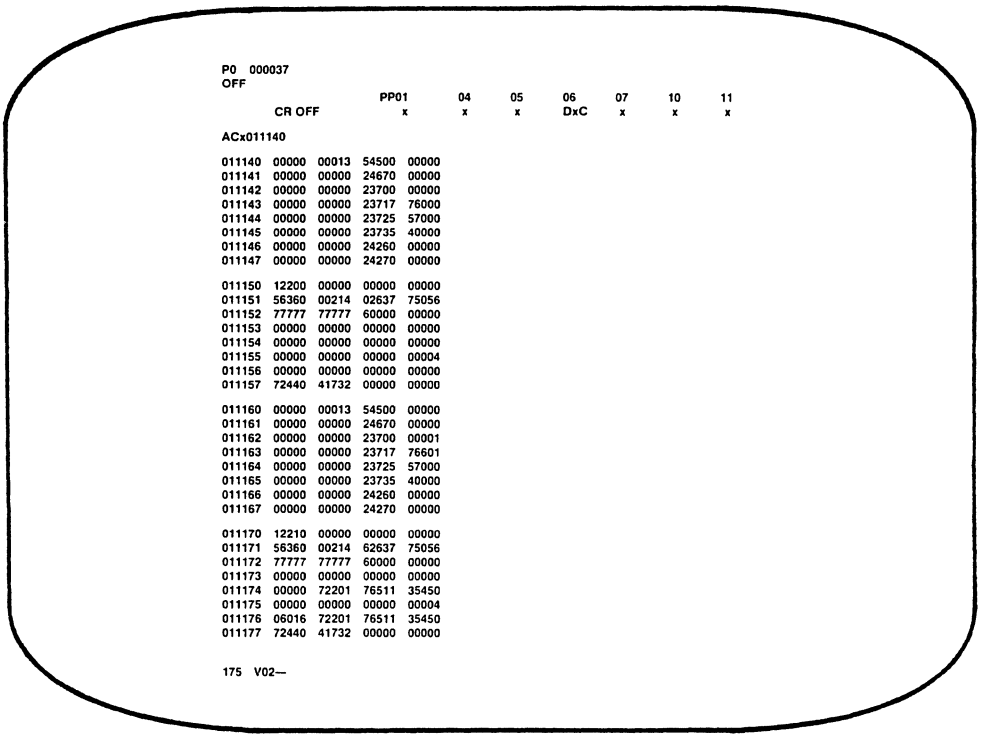
```
        EM (NONE)
        CM (  65K)
CH00    01      02      03      04      05      06      07      10      11      12      13      A  0000
  —     P00     E00     E       —00     —       —       P       E       —       —       —

    CT3  005555

MODE  RUN               AVAILABLE FL        150777
BKP                     EXCHANGE RATE       0500

 0 CT3    P  005555             EX  010040
          RA  010000             FL  017000
    PC  00028555                                        EC  0000
```

Reference #1



```
P0  000037
OFF
                                PP01      04      05      06      07      10      11
          CR OFF                  x       x       x      DxC      x       x       x

ACx011040

011040  00000  00000  00000  00000
011041  00000  00000  00000  00000
011042  00000  00000  00000  00000
011043  00000  00000  00000  00000
011044  00000  00000  00000  00000
011045  00000  00000  00000  00000
011046  00000  00000  00000  00000
011047  00000  00000  00000  00000

011050  00000  00000  00000  00000
011051  00000  00000  00000  00000
011052  00000  00000  00000  00000
011053  00000  00000  00000  00000
011054  00000  00000  00000  00000
011055  00000  00000  00000  00000
011056  00000  00000  00000  00000
011057  00000  00000  00000  00000

011060  00000  00000  00000  00061
011061  00000  00000  23700  00060
011062  00000  00000  23700  00001
011063  00000  00000  00000  01142
011064  00000  00000  00000  01162
011065  00000  00000  00000  00000
011066  00000  00000  00000  00000
011067  00000  00000  00000  00000

011070  00000  00000  00000  00000
011071  00000  00000  00000  00000
011072  00000  00000  00000  00000
011073  00000  00000  00000  00000
011074  00000  00000  00000  00000
011075  00000  00000  00000  00000
011076  00000  00000  00000  00000
011077  00000  00000  00000  00000


173 V02—
```

Reference #2



```
P0  000037
OFF
                          PP01      04      05      06      07      10      11
        CR OFF              x       x       x      DxC      x       x       x

ACx011140

011140  00000  00013  54500  00000
011141  00000  00000  24670  00000
011142  00000  00000  23700  00000
011143  00000  00000  23717  76000
011144  00000  00000  23725  57000
011145  00000  00000  23735  40000
011146  00000  00000  24260  00000
011147  00000  00000  24270  00000

011150  12200  00000  00000  00000
011151  56360  00214  02637  75056
011152  77777  77777  60000  00000
011153  00000  00000  00000  00000
011154  00000  00000  00000  00000
011155  00000  00000  00000  00004
011156  00000  00000  00000  00000
011157  72440  41732  00000  00000

011160  00000  00013  54500  00000
011161  00000  00000  24670  00000
011162  00000  00000  23700  00001
011163  00000  00000  23717  76601
011164  00000  00000  23725  57000
011165  00000  00000  23735  40000
011166  00000  00000  24260  00000
011167  00000  00000  24270  00000

011170  12210  00000  00000  00000
011171  56360  00214  62637  75056
011172  77777  77777  60000  00000
011173  00000  00000  00000  00000
011174  00000  72201  76511  35450
011175  00000  00000  00000  00004
011176  06016  72201  76511  35450
011177  72440  41732  00000  00000

175  V02—
```

Reference #3

LEARNING ACTIVITY 11-F. EXERCISE: CT3 DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic CT3 in learning activity 11-E.

OBJECTIVE

- You will be able to describe the purpose of CT3; describe the parameters required to execute CT3; and describe the results expected (normal and abnormal) from the execution of the diagnostic CT3.

Directions: The following questions refer to the description and use of the diagnostic CT3. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. An error is detected by CT3 when the computed answer does not compare with the machine answer.

2. What is the result of setting the following locations as follows?

   Loc. 12 (Relative) = 1
   Loc. 13 (Relative) = 40
   Loc. 14 (Relative) = 41

   only 40 and [illegible]

3. List the four options available when CT3 detects an error.

   [illegible]
   Stop
   [illegible]
   [illegible]

4. It is desirable to begin execution of CT3 at pass count 4,721,342$_8$. How is this accomplished? RA + 2 = 4,721,342$_8$

5. List the two different error types detected and defined by CT3. Register error Checksum error

6. It should be assumed that the simulator answer is always the correct answer. True or False? Explain your answer.

False 99% simulation correct

7. The documentation for CT3 states that machine and simulated answers are stored in Central Memory in exchange package format. What is exchange package format?

answers stored as exchange package

8. In the case of an error, all of the pertinent information is found in memory, such as machine and simulator answers failing register, and error conditions. How do you determine the failing instruction?

Examine the failing registers as a result

9. Random numbers are used for instructions only. Operands are "fixed" by the test itself. True or False?

False

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 11-F

1. Machine, simulator (or vice-versa)

2. Only 40XXX and 41XXX instructions will occur in the random loop.

3. a. Dump and continue
   b. Stop
   c. Loop on error
   d. Loop on error, and stop when error recurs

4. Enter memory location RA+2 with the number 4721342_8.

5. Register error, checksum error.

6. False. In the vast majority of the cases, the simulated answer is the correct one. However, because CT3 utilizes a CPU simulator, there is a remote possibility of simulator error.

7. Exchange package format means that when the either the CPU or the simulator completes execution of a random loop, the resulting answers are stored in memory to look exactly like an exchange package.

8. The random instruction loop is located at RA+600 in central memory. The instructions should be examined to locate one which used the same result register as the failing register from the exchange packages. Careful examination of this instruction and preceding ones should lead to the failing one.

9. False. Both instructions and operands are formed from the random number generator output.

LEARNING ACTIVITY 11-G. REFERENCE READING: CU1 DESCRIPTION

During this activity you will learn about the diagnostic CU1.

OBJECTIVE

- You will be able to describe the purpose of CU1; describe the parameters required to execute CU1; and describe the results expected (normal and abnormal) from the execution of the diagnostic CU1.

Directions: Read the CU1 description included in the next few pages of this learning activity.

Also locate the central processor test 1 (CU1) description found in the 6000/CYBER 70/CYBER 170 System Mainteance Monitor (SMM) Reference Manual, volume 3, publication number 60160600. Become familiar with the information on pages CU1-1 through CU1-5.

When you feel comfortable with your understanding of CU1 proceed to learning activity 11-H. In learning activity 11-H you will be answering questions designed to reinforce your ability to comprehend the description and use of CU1.

CU1 Description

CU1 or central processor test 1 is a basic CPU command test. Its purpose is to verify the CPUs ability to correctly execute instructions. CU1 utilizes canned operands to perform a check of the CPU control hardware (branch) and the large and small arithmetic sections. Before running CU1 the PPS and CSU chassis must be verified. CU1 does not sense parity or SECDED errors nor does it execute any random instruction sequences.

CU1 should be executed under EXC control. To do this, load EXC first and then use the EXC load command to load CU1. EXC will create the exchange packages and control the test execution.

CU1 is a CPU program and it resides in central memory. It uses the first 6300_8 addresses in CM. The test uses fixed operands and instructions and will repeat itself until stopped by the user. The test is broken down into small sections of code, each section testing one instruction or operation. Each section is separated by CPU stop codes (stop code=000------000). If a particular section

executes correctly the program will branch around the stop code and execute the next section. If an error is detected the program will execute the stop instruction.

There are no running/error displays for CU1 other than the EXC display. If the CPU P register is changing, CU1 is executing properly. If an error occurs P will stop and the stop address will point to the section of failing code.

In the case of an error condition (P stopped), look up the error stop address in central memory or the actual program listing. If the error stop is not legal suspect a PPS or central memory problem and take appropriate action. When a legal error stop occurs perform the following:

a. By consulting the succeeding list, determine the general failing instruction type.
b. Display the group of instruction preceding the error stop.
c. By viewing these instructions, it may be possible to isolate the exact instructions and the failing bit(s).
d. The following is an example of the preceding:
error stop - P = 01017
from list - failing instruction type = long add X_k
display memory from 1010-1020 =

```
1010 - 00000 00000 00000 00000 - Error stop from last loop.
1011 - 71000 00001 10300 46000 - X0 & X3 = 01
1012 - 36303 20301 36103 20101 - X3 = 4, X1 = 12
1013 - 36401 20401 36604 20601 - X4 = 26, X6 = 56
1014 - 36506 20501 36705 20701 - X5 - 136, X7 = 276
1015 - 36207 20201 36002 20001 - X2 - 576, X0 = 1376
1016 - 72007 76401 03000 01020 - X0 should = 0000
1017 - 00000 00000 00000 00000 - Error Stop X0 ≠ 0
1020 - Start next section
```

By proper breakpointing, the 60 bit word which is producing the failure can be determined. For example, a breakpoint at M.L. 1014 should result in X4=26 and X6=56. If not, a failure has occurred in a previous 60 bit word. Breakpoint farther back in the program. Restart CU1 and check again.

NOTE

As of this writing, 4/83, the error stop addresses in the CU1 documentation (CU1 microfiche) are off by 100_8 locations. To get the actual stop address add 100_8 to the listed address (that is, Under the "Test Read Flags Section", Increment Xj test should start at location 425_8).

LEARNING ACTIVITY 11-H. EXERCISE: CU1 DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic CU1 in learning activity 11-G.

OBJECTIVE

- You will be able to describe the purpose of CU1; describe the parameters required to execute CU1; and describe the results expected (normal and abnormal) from the execution of the diagnostic CU1.

Directions: The following questions refer to the description and use of the diagnostic CU1. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. What is the purpose of the CU1 diagnostic program? _____

2. List the procedure which should be used to load CU1 when using SMM. _____

3. Which area of the mainframe must be verified before running CU1? _____

4. What is the indication that CU1 is executing properly? _____

5. What happens if CU1 detects an error? _____

6. While running CU1 under EXC control the CPU P register stops at address 2771$_8$. Which CPU data path is failing? _____

7. What should you do if CU1 consistently stops at other than a legal error address? _____

ANSWERS FOR LEARNING ACTIVITY 1-H

1. The CU1 diagnostic program is a fixed operand CPU instruction test.

2. CU1 should be run under the control of EXC. Therefore, to load CU1 you should first load EXC and then use an EXC load command to load CU1.

3. The PPS chassis and central memory.

4. The CPU P register should be changing when CU1 is executing properly.

5. The CPU will execute a 00 instruction and stop. EXC will display the contents of the CPU P register.

6. The failing path is either to or from X0.

7. You should verify the PPS chassis central memory.

LEARNING ACTIVITY 11-I. REFERENCE READING: MAN DESCRIPTION

During this activity you will learn about the diagnostic MAN. A microfiche viewer will be required for portions of this activity.

OBJECTIVE

- You will be able to describe the purpose of MAN; describe the parameters required to execute MAN; and describe the results expected (normal and abnormal) from the execution of the diagnostic MAN.

Directions: Read the MAN description included in the next few pages of this learning activity. A microfiche titled "MAN Diag. Prog Listings" will be utilized in this description.

Also locate the monitor related exchange jump diagnostics (CEJ/MEJ/MAN/EEJ/ZEJ) description found in the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, volume 2, publication number 60160600. Become familiar with the information on pages MAN-1 through MAN-63.

When you feel comfortable with your understanding of MAN proceed to learning activity 11-J. In learning activity 11-J you will be answering questions designed to reinforce your ability to comprehend the description and use of MAN.

INTRODUCTION TO MAN

The MAN diagnostic was written to check out the monitor exchange jump circuits of the CYBER 170. The basic exchange jumps are checked by the test, EJT. Remember that there are two types of monitor exchange jumps from the PP. One type (MXN) uses the contents of the A register in the PP for the exchange address. The second type (MAN) uses the contents of the MA register in the CPU for the exchange address. Both types are dependent on the monitor flag in the CPU = perform the exchange if the flag is clear, pass if the flag is set.

The CPU monitor exchange circuits are also tested. Once again there are two types. One type occurs when the monitor flag is set and the second type when the flag is clear. The difference being the source of the exchange address; Bj+k and MA respectively. Proper central exchange jump responses to error conditions is also verified by the MAN test.

The MAN test uses fixed patterns of data for its exchange package information. Various addresses within central memory are used for exchange addresses, thus checking for exchanging to the proper place in central memory. Exchanges are attempted with the monitor flag both cleared and set. Following the execution of each exchange instruction the CPU P register and exchange package contents are checked for correct data. If the flag was set and a PP monitor exchange jump was executed, a check is made to verify that the attempted exchange did not occur. The CPU is used to clear the monitor flag once it has been set via a PP monitor exchange.

Using MAN

The purpose of this section is to alert you to any pitfalls of this test and give any pointers that may be helpful in using it.

1. Before running the MAN test, be certain ERX and EJ1 both execute without error. False errors can result if these tests do not run.

2. MAN will execute only under the multiprogramming (AUTO) scheme.

3. Make sure the CEJ-MEJ switch on the deadstart panel is switched on.

4. MAN should not be run when other programs which use the CPU or central memory are being run.

5. In the case of an error, setting locatio 1501 of the PP=4X11 will result in a repeat condition with nothing being displayed. A tight scoping loop will result, however as MAN does not commmunicate with CPC and LDR, control will be lost and a deadstart will be required to restart.

MAN Documentation

At this time locate the microfiche titled, "MAN Diag. Prgm Listings", and insert it in the viewer. Position the viewer at grid location B1 which should correspond to page 1 of the listing. Find the beginning of the documentation section of the listing (usually within the first 4 pages). Review the documentation paying particular attention to basic philosophy, parameters, commands, and display information.* Gain an understanding of the general concepts before

* If you are not familiar with the general organization of a Compass listing, refer to page 11-57 and 11-58.

looking at detailed flowcharts and section descriptions. Try to determine general flow of the test including testing sequence, PPUs and channel used, central memory usage and PPU/CPU residence.

NOTE

When you are through studying the MAN documentation on the microfiche, return to this activity and continue reading at the next topic, MAN Displays.

MAN Displays

We will now look at some actual MAN displays. These displays were made from photographs taken of a CYBER 170 display console. The purpose of these displays is to familiarize you with the actual running/error displays for the diagnostic. Your success or failure in using MAN effectively will depend largely on whether or not you an correctly interpret the information presented on these displays.

Reference #1 - MAN Parameter Display

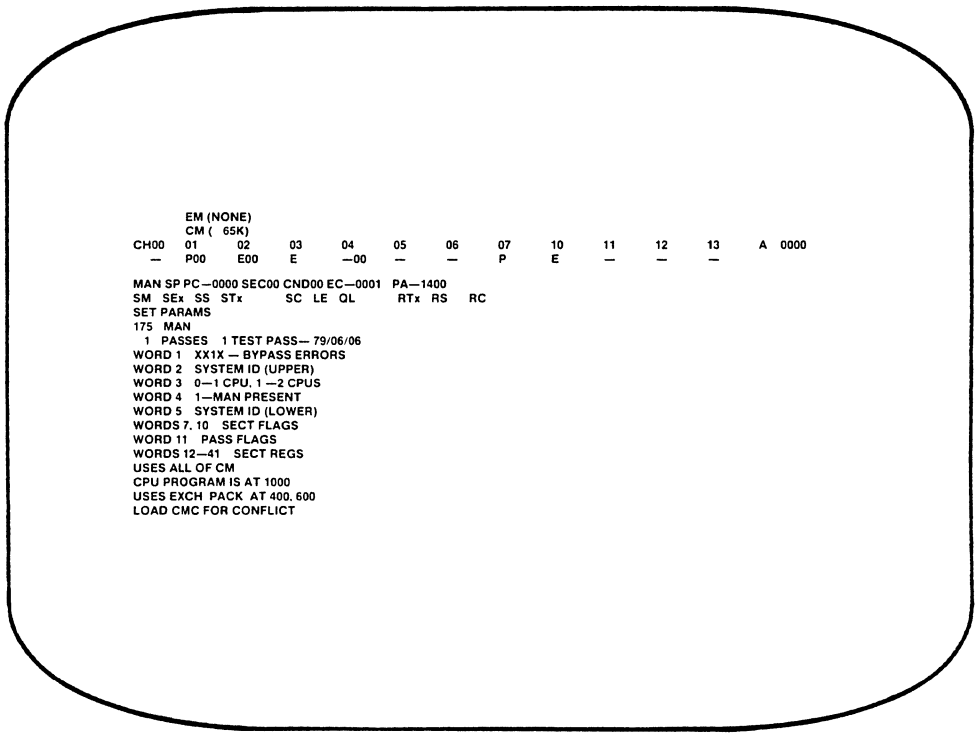
This is a picture of the MAN test parameter entry dispay. You will notice that all select parameters such as stop-on-error(s) are noted with an asterisk. The MAN CPU program is at Central Memory location 1000. These parameters will be located at memory location 1500-1550 in the PP containing MAN. If MAN was loaded into PP6, parameter word 3 could be modified with the entry 6.1503,XXXX.

Reference #2 - MAN Running Display

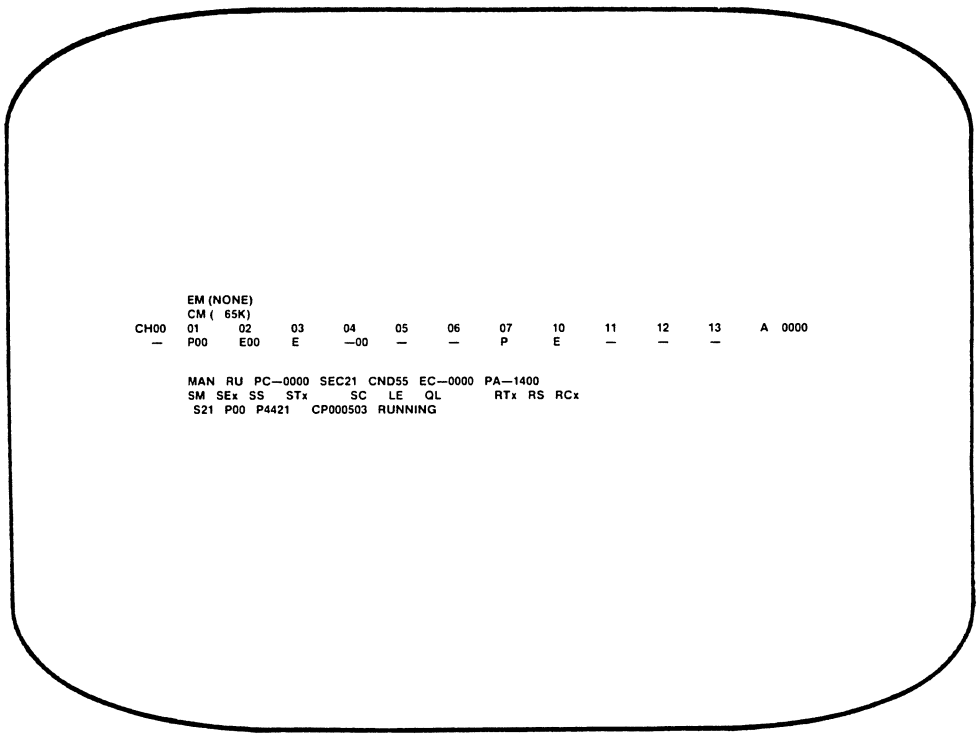
When MAN is running, this information will be being displayed. The first line contains the pass count (PC), the section number currently running (SEC XX), the current condition (CNDXX), the error count (EC), and the parameter table first word address. The second line contains the selected options. The third line contains the section number, pattern number (PXX), PP and CPU P registers.

Reference #3 - MAN Error Display

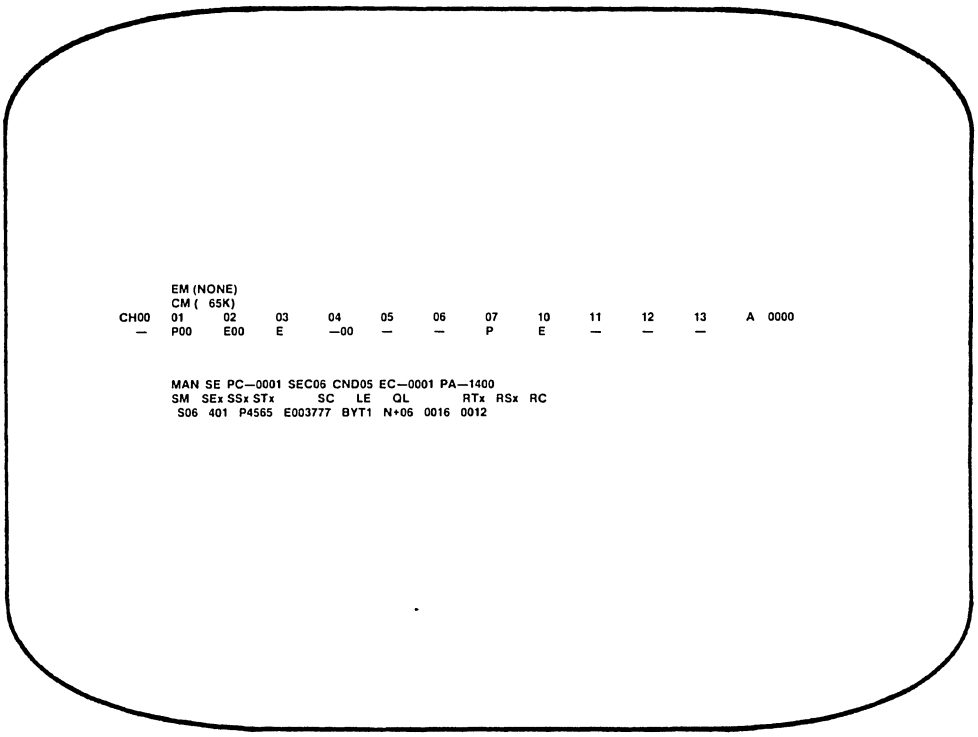
The primary differences between this and the running display are on the third line. The second number (401) is the error code, followed by the P register address, the current output exchange package address, and the information concerning the error. This error is in byte 1, word 6 of the exchange package, and indicates a dropped bit.



Reference #1



Reference #2


EM (NONE)
CM (65K)
CH00 01 02 03 04 05 06 07 10 11 12 13 A 0000
— P00 E00 E —00 — — P E — — —
MAN SE PC—0001 SEC06 CND05 EC—0001 PA—1400
SM SEx SSx STx SC LE QL RTx RSx RC
S06 401 P4565 E003777 BYT1 N+06 0016 0012

Reference #3

LEARNING ACTIVITY 11-J. EXERCISE: MAN DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic MAN in learning activity 11-I.

OBJECTIVE

- You will be able to describe the purpose of MAN, describe the parameters required to execute MAN, and describe the results expected (normal and abnormal) from the execution of the diagnostic MAN.

Directions: The following questions refer to the description and use of the diagnostic MAN. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. Test MAN checks out the exchange on zero (Halt) instruction. True or False? TRUE

2. The MAN test has two individual parts. Name the two parts and briefly describe each. MAN MCN

3. A failure occurs, the error code equals 022. In which of the five possible formats will the error information be displayed? E

4. MAN is executing in a CPU with 131K of memory available. Central Memory address 525252 will be used as an output exchange package address. True or False? Why? FALSE
131 K 000016

The answers for this learning activity are on the following page.

ANSWERS FOR LEARNING ACTIVITY 11-J

1. True

2. Part 1: MAN - PP portion of test responsible for overall control.
   Part 2: MNC - CPU portion performs central exchanges to control the monitor flag and test CEJ instructions.

3. Error information will be displayed in format E.

4. False. This address is too large for a 131K machine.

LEARNING ACTIVITY 11-K. REFERENCE READING: ERX DESCRIPTION

During this activity you will learn about the diagnostic ERX. A microfiche viewer will be required for portions of this activity.

OBJECTIVE

- You will be able to describe the purpose of ERX; describe the parameters required to execute ERX; and describe the results expected (normal and abnormal) from the execution of the diagnostic ERX.

Directions: Read the ERX description included in the next few pages of this learning activity. A microfiche titled "ERX Diag. Prog. Listings" will be utilized in this description.

Also locate the Error Exit Test (ERX) description found in the 6000/ CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, volume 2, publications number 60160600. Become familiar with the information on pages ERX-1 through ERX-15.

When you feel comfortable with your understanding of ERX, proceed to learning activity 11-L. In learning activity 11-L you will be answering questions designed to reinforce your ability to comprehend the description and use of ERX.

INTRODUCTION TO ERX

The ERX diagnostic is available to test the error exit circuits in the 170 CPU. The error exit circuits handle four basic types of hardware exit conditions. These are: arithmetic errors, (infinite and indefinite), address out of range, ECS exit cases, and illegal instructions.

ERX checks the exit circuits by executing a small program in the CPU. This program is only one central memory word in length followed by a stop instruction = 56600 00000. This stop instruction loads the contents of RA into register X6 and halts. Keep in mind that when an error exit does occur, the information concerning the error (contents of P register and exit mode bit) are written by the hardware into RA. An exchange jump is executed and the CPU program executes the PP containing the ERX diagnostic then checks RA to verify that the error exit did or did not occur. Depending upon the operands used for input to the instruction under test, an error exit may be expected or it may not. By using different input operands and an error mode of either 0 or 7, ERX can check for all combinations of error exits.

The multiply, divide, floating add, and normalize functional units are checked. In addition to checking for the proper error exit condition, ERX also verifies that central memory is not modified when an error exit producing or an illegal instruction is executed. This is done by filling all of central memory to a pattern, and then checking the pattern following execution of the instruction under test. On each pass through ERX, the RA of the central memory program is updated and after about a dozen passes the entire available central memory will have been used. An input parameter may be modified to inhibit this automatic updating.

ERX cannot be run with other tests also executing. It may be run stand-alone and also under control of SMM Auto mode. It cannot be executed under control of EXC.

Using ERX

The purpose of this section is to alert you to any pitfalls of the test and give any pointers that may be helpful in using it.

1. ERX cannot be executed under control of EXC.

2. In order to prevent false errors, make certain the PPS, CM, and the CPU are operational.

3. Make certain that the parameters at MCP2, MCP3, and MCP4 are properly set before running, or false errors may result.

4. When an error occurs, carefully note the instructions, operands, and the setting of the EM register. This information can be used to duplicate the failure.

5. If an error occurs with the same RA, try running ERX with an RA set in MCP7 and MCP10. This will eliminate any false error which is caused by a memory failure.

ERX Documentation

At this time locate the microfiche titled "ERX Diag. Prgm Listings", and insert it in the viewer. Position the viewer at grid loation B1 which should correspond to page 1 of the listing. Find the beginning of the documentation section of the listing (usually within the first four pages). Review the documentation paying particular attention to basic philosophy, parameters, commands, and display

information.* Gain an understanding of the general concepts before looking at detailed flowcharts and section descriptions. Try to determine general flow of the test including testing sequence, PPUs and channel used, central memory usage, and PPU/CPU residence.

NOTE

When you are through studying the ERX documentation on the microfiche, return to this activity and continue reading at the next topic, ERX displays.

ERX Displays

We will now look at some actual ERX displays. These displays were made from photographs taken of a CYBER 170 display console. The purpose of these displays is to familiarize you with the actual running/error displays for the diagnostic. Your success or failure in using ERX effectively will depend largely on whether or not you an correctly interpret the information presented on these displays.

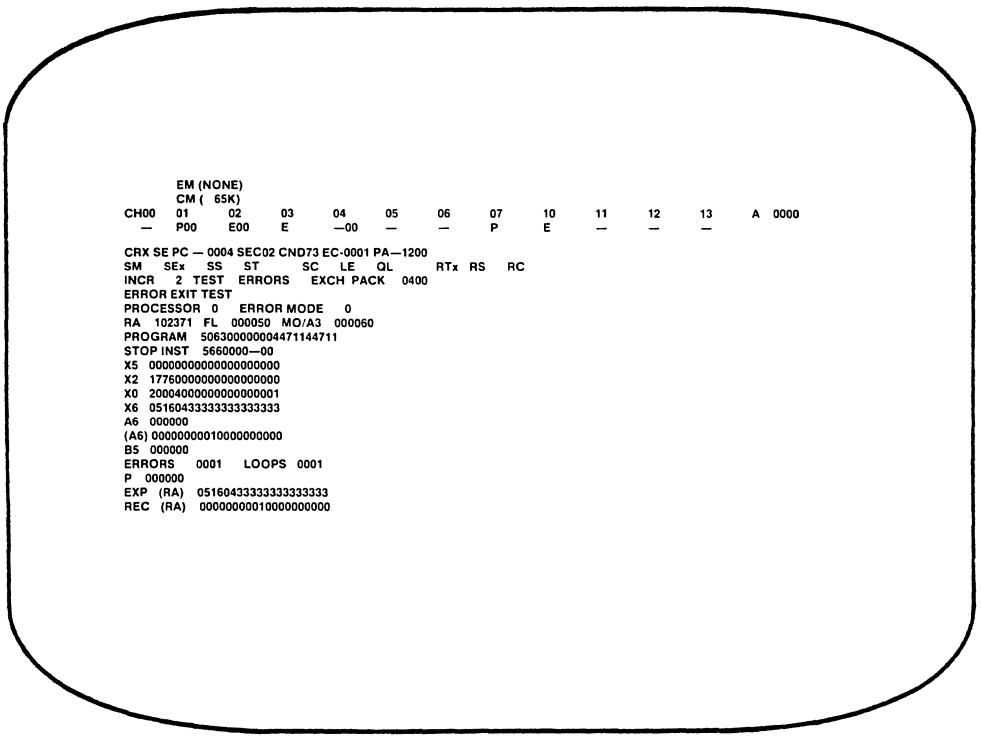
Reference #1 - ERX Parameter Display

This is a picture of the ERX initial display. As you can see the first three lines are almost identical with the previous example. Note, however, that the parameters begin at location 1200 in the PP. The parameters are explained in the MSL reference manual and may be modified using the standard keyboard commands.

Reference #2 - ERX Error Display

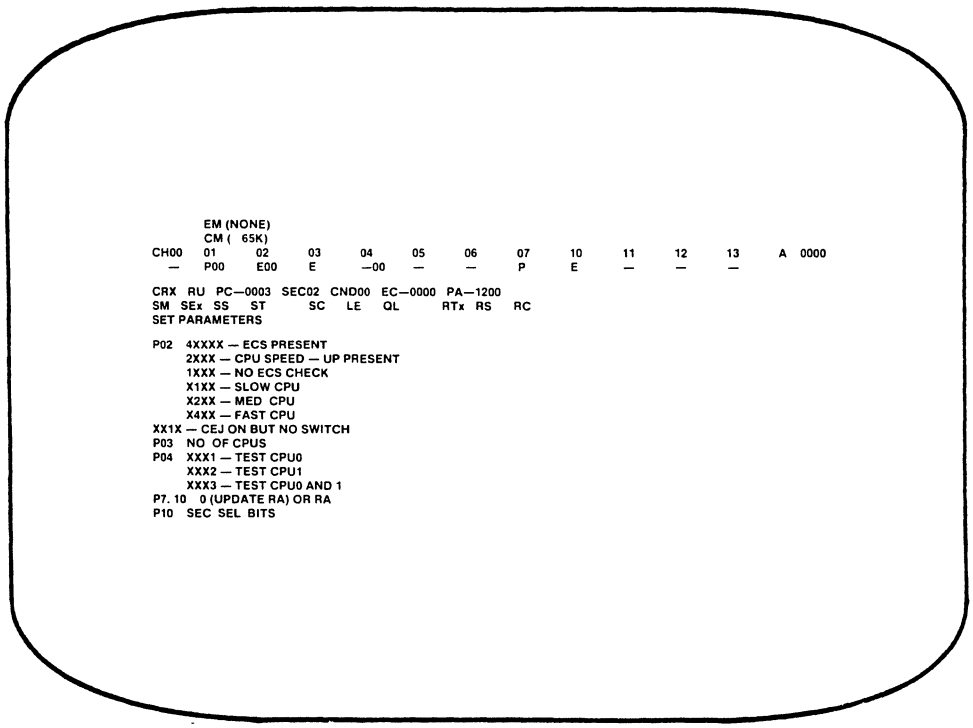
The error information begins on line 3. All pertinent information is given. This error is an error in the increment test portion of the test. All lines of the error display are explained in the reference manual. This information will not be re-explained here. Normal procedure would be to record this information then run farther or rerun and check for a duplicate error or another failure of the same type.

* If you are not familiar with the general organization of a Compass listing, refer to page 11-57 and 11-58.



```
        EM (NONE)
        CM (  65K)
CH00    01      02      03      04      05      06      07      10      11      12      13      A  0000
  —     P00     E00     E       —00     —       —       P       E       —       —       —

CRX SE PC — 0004 SEC02 CND73 EC-0001 PA—1200
SM   SEx   SS   ST      SC   LE   QL      RTx  RS   RC
INCR   2  TEST  ERRORS   EXCH PACK   0400
ERROR EXIT TEST
PROCESSOR  0    ERROR MODE   0
RA  102371  FL  000050  MO/A3  000060
PROGRAM  506300000004471144711
STOP INST  5660000—00
X5  0000000000000000000
X2  17760000000000000000
X0  20004000000000000001
X6  05160433333333333333
A6  000000
(A6) 00000000010000000000
B5  000000
ERRORS   0001   LOOPS  0001
P  000000
EXP  (RA)  0516043333333333333
REC  (RA)  0000000010000000000
```

Reference #2



```
        EM (NONE)
        CM (  65K)
CH00    01      02      03      04      05      06      07      10      11      12      13      A  0000
  —     P00     E00     E       —00     —       —       P       E       —       —       —

CRX  RU  PC—0003  SEC02  CND00  EC—0000  PA—1200
SM  SEx  SS   ST      SC   LE   QL      RTx  RS   RC
SET PARAMETERS

P02  4XXXX — ECS PRESENT
     2XXX — CPU SPEED — UP PRESENT
     1XXX — NO ECS CHECK
     X1XX — SLOW CPU
     X2XX — MED  CPU
     X4XX — FAST CPU
XX1X — CEJ ON BUT NO SWITCH
P03  NO  OF CPUS
P04  XXX1 — TEST CPU0
     XXX2 — TEST CPU1
     XXX3 — TEST CPU0 AND 1
P7. 10   0 (UPDATE RA) OR RA
P10  SEC  SEL  BITS
```

Reference #1

LEARNING ACTIVITY 11-L. EXERCISE: ERX DESCRIPTION REVIEW

This activity reinforces what you learned about the diagnostic ERX in learning activity 11-K.

OBJECTIVE

- You will be able to describe the purpose of ERX, describe the parameters required to execute ERX, and describe the results expected (normal and abnormal) from the execution of the diagnostic ERX.

Directions: The following questions refer to the description and use of the diagnostic ERX. Answer these questions and then check your answers with the correct answers provided at the end of this activity.

1. The ERX test does not have the built-in ability to loop on an error. True or False? Explain your answer. FALSE, SET (5 0)

2. During its normal testing sequence, ERX checks for two basic problems. List them. [illegible]

3. List three possible causes of an error exit. [illegible]

4. The following instruction, 46700, is illegal on a CYBER 720/730. True or False? FALSE

5. ERX checks for exit conditions by using two different settings of the EM register. List and explain these two settings. [illegible]

ANSWERS FOR LEARNING ACTIVITY 11-L

1. False. ERX can loop on an error by setting the appropriate repeat bit in parameter word MCP.

2. Improper handling of error conditions and incorrect modification of central memory.

3. Arithmetic errors - indefinite, infinite
   Illegal instructions
   Address out of range

4. False

5. EM = 0 Do not stop on an error condition.
   EM = 7 Stop on all possible error exit conditions.

LEARNING ACTIVITY 11-M. REFERENCE READING: COMPARE/MOVE UNIT DIAGNOSTIC DESCRIPTION

During this activity you will learn about the compare/move unit diagnostics CMS and BD1/BDP. A microfiche viewer will be required for portions of this activity.

OBJECTIVE

- You will be able to describe the purpose of CMS and BD1/BDP, describe the parameters required to execute CMS and BD1/BDP, and describe the results expected (normal and abnormal) from the execution of the diagnostics CMS and BD1/BDP.

Directions: Read the CMS and BD1/BDP descriptions included in the next few pages of this learning activity. A microfiche titled "CMS Diag. Prog. Listings" will be utilized in the description of CMS. Microfiche titled "BD1 Diag. Prog. Listings" and "BDP Diag. Prog. Listings" will be utilized in the description of BD1/ BDP.

Locate the compare/move instruction tests (BD1/BDP) description found in the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, volume 2, publication numbers 60160600. Become familiar with the information on pages BD1-1 through BD1-54.

Also locate the random compare/move unit test (CMS) description found in the 6000/CYBER 70/CYBER 170 System Maintenance Monitor (SMM) Reference Manual, volume 2, publication numbers 60160600. Become familiar with the information on pages CMS-1 through CMS-54.

When you feel comfortable with your understanding of CMS and BD1/BDP proceed to learning activity 11-N. In learning activity 11-N you will be answering questions designed to reinforce your ability to comprehend the description and use of CMS and BD1/BDP.

INTRODUCTION TO CMU TESTS

There are two basic tests available for testing the compare-move unit. One of these tests is named CMS. This test executes in the CPU and does not communicate directly with any PPU. CMS has six basic sections which check moves, compares, and addressing. This test uses a random number generator to obtain random numbers for use as descriptors and operands. It is possible to change the starting random number and therefore the descriptors and operands used in the test. Because random numbers are used, there is always the possibility of running into a failing combination.

The second diagnostic for testing the compare-move hardware is BDP/BD1. This diagnostic has two unique components: BD1 is a PPU program, while its CPU component is named BDP. The PPU program is responsible for controlling the CPU program. The CPU program (BDP) is the actual test for the CMU. It contains the parameter words, and error and pass counters as well as the actual test program. This test uses fixed operands and instructions which allow for better pinpointing of any problems which might occur. In addition to direct and indirect moves and collated and uncollated compares, address out of range, exchange jump and memory conflicts, the K2+RA adder, and the shift network and move data path are tested.

Using CMS and BDP/BD1

The purpose of this write-up is to alert you to any pitfalls of these tests and give any pointers that may be helpful in using them.

1. Because BD1/BDP uses fixed or canned numbers, it should normally be run before CMS.

2. Make certain that the PPS command and memory tests, the CPU command and memory tests, and the exchange jump tests all run before attempting to check out the compare-move circuitry.

3. Because CMS is a fast running test, it is ideally suited for execution during shock testing the CMU.

4. CMS does not generate a display, therefore when an error occurs it will stop with P=304. It will be necessary to check central memory to determine the failure. The location of the error information is defined in the program listing.

5. In the case of a solid failure, use BD1/BDP to isolate the failure.

6. If possible, run BD1/BDP by using a PP. This would be called in using an X.BD1 command under SMM. BD1 will load BDP and halt for parameter changes. The RA of the test in central memory will depend upon which PP the BD1 portion is loaded into. For example: If BD1 is loaded into PP4, BDP will be loaded into central memory beginning at location 41000 (absolute), if into PP5 then at central memory 51000, and so forth. When BD1/BDP is called and used this way, any error will result in an error display.

7. BDP can be executed under control of EXC. This method is less desirable, as no error displays are produced upon failure. The program will halt with an error and display a passcount, error count, and a one line message.

CYBER 170 Model 720/730 CPU
Learning Activity 11-M

CMU Test Documentation

At this time locate the microfiche for the CMU Tests (CMS Diagnostic Program Listing and BD1/BDP Diagnostic Program Listing) titled CMU Test Diag. Prgm Listings, and insert it in the viewer. Position the viewer at grid location B1 which should correspond to page 1 of the listing. Find the beginning of the documentation section of the listing (usually within the first four pages). Review the documentation paying particular attention to basic philosophy, parameters, commands, and display information.* Gain an understanding of the general concepts before looking at detailed flowcharts and section descriptions. Try to determine general flow of the test including testing sequence, PPUs and channel used, central memory usage, and PPU/CPU residence.

NOTE

When you are through studying the CMU Test documentation on the microfiche, return to this activity and continue reading at the next topic, CMU Test Displays.

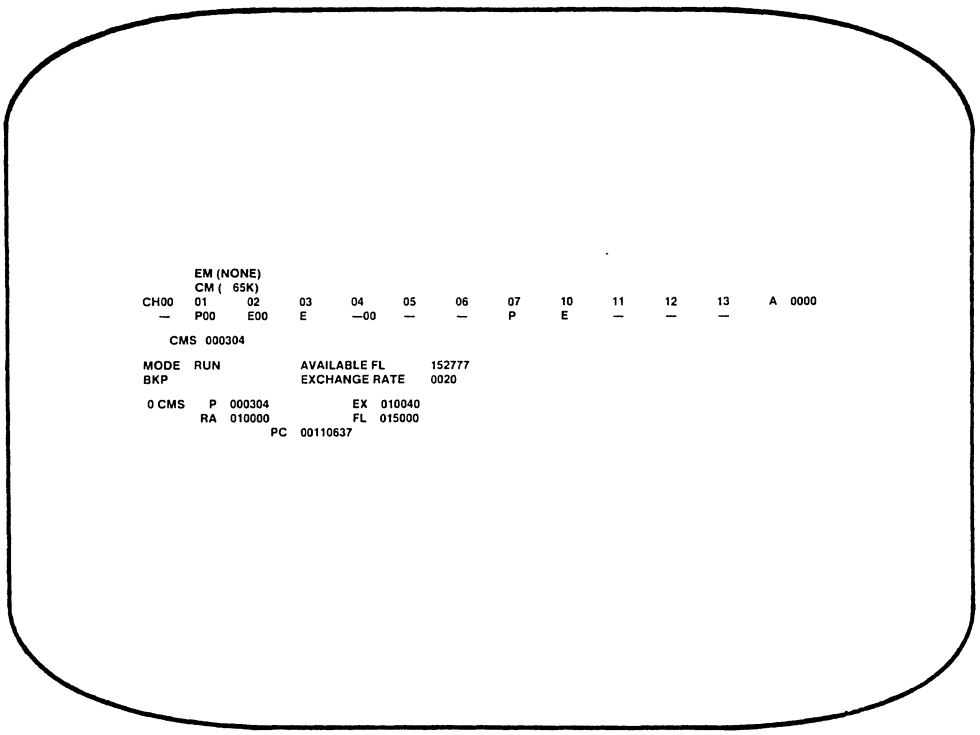
CMU Test Displays

We will now look at some actual CMU test displays for CMS and BD1/BDP. These displays were made from photographs taken of a CYBER 170 display console. The purpose of these displays is to familiarize you with the actual running/error displays for the diagnostic. Your success or failure in using CMS and BDP effectively will depend largely on whether or not you an correctly interpret the information presented on these displays.

* If you are not familiar with the general organization of a Compass listing, refer to page 11-57 and 11-58.

Reference #1 - CMS Error Display

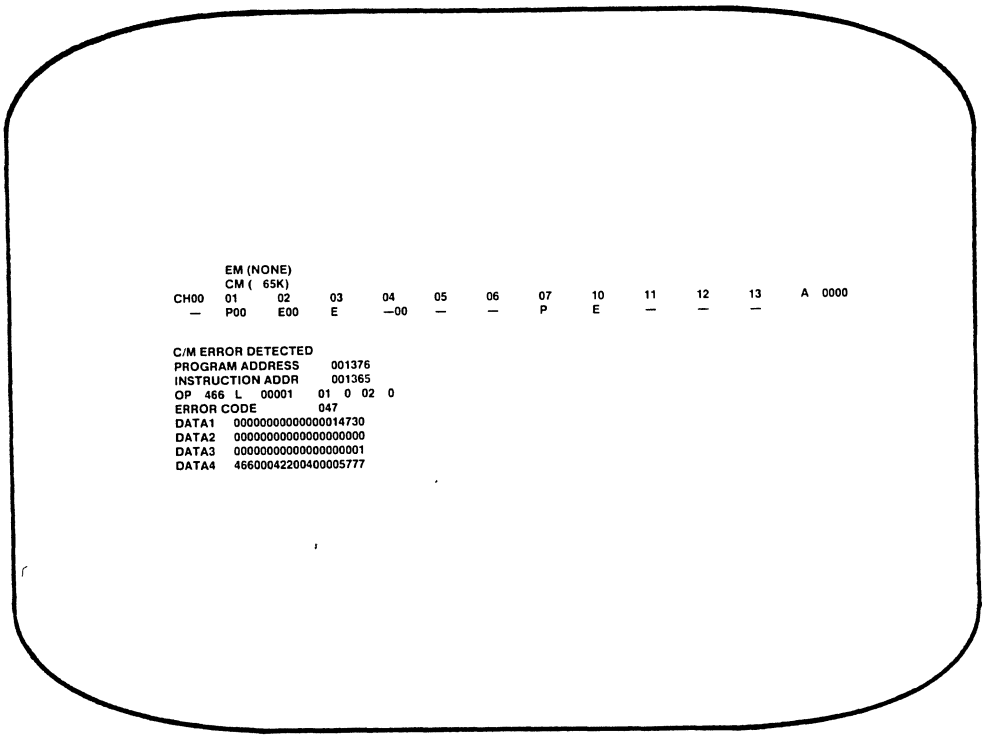
The attached error display is a result of an error detected by CMS while running under control of EXC. The CMS test has no additional error display. The test simply halts with the P register equal to 304. In order to determine the error, it would be necessary to check the contents of memory (beginning at RA=10000 for this failure). A listing of CMS would be required to determine the exact failure.



Reference #1 - CMS Error Display

Reference #2 - BDP Error Display

The attached display would appear in the case of a problem detected by BD1. The location of the instruction is given. The instruction is also broken down into its primary parts such as OP code, L, and offsets. The meaning of the contents of each of the data registers is dependent upon the particular error code. For this example, with an error code = 047, data 1 = (A0), collate table address, data 2 = expected X0 result, data 3 = actual X0 result, and data 4 = failing instruction. So for this example, bit 0 is failing.



Reference #2 - BDP Error Display

LEARNING ACTIVITY 11-N. EXERCISE: COMPARE/MOVE UNIT DIAGNOSTIC DESCRIPTION REVIEW

This activity reinforces what you learned about the compare/move unit diagnostics CMS and BD1/BDP in learning activity 11-M.

OBJECTIVE

- You will be able to describe the purpose of CMS and BD1/BDP, describe the parameters required to execute CMS and BD1/BDP, and describe the results expected (normal and abnormal) from the execution of the diagnostics CMS and BD1/BDP.

Directions: The following questions refer to the description and use of the diagnostics CMS and BD1/BDP. Answer these questions and then check your answers with the correct answers provided at the end of this section.

1. With BDP loaded into central memory, what information will be found in relative memory location 00003? _____

2. The test CMS uses random operands and fixed or canned descriptors. True or False? Explain your answer. _____

3. Explain the principal difference between BD1 and BDP. _____

4. It is possible to run BDP without BD1. True or False? Explain. _____

5. When an error occurs (BD1/BDP) an error code will be displayed along with other information concerning the error. Where can information concerning the error code be found? _____

6. With test CMS executing, how can the pass number of the current pass be determined? _____

ANSWERS FOR LEARNING ACTIVITY 11-N

1. Location 3 contains the section select bits and will contain either 0317 or 0217 depending upon how BDP is loaded.

2. False. Both operands and descriptors are generated randomly.

3. BD1 is a PPU program for control of BDP which is a CPU program doing the actual testing.

4. True. BDP can be run under control of EXC.

5. Error code information is available from either the SMM Reference Manual, Vol. 2, or the test documentation on microfiche.

6. The pass number is located in central memory relative location 205.

BASIC CONTENTS OF A COMPASS LISTING

Effective immediately, the documentation for all diagnostics is included in the source code. There will no longer be any separate reference manual with information in the individual tests. This makes it necessary for the CE to look at a compass program listing in order to find the documentation required.

This is a brief description of the contents of a typical program listing. In general, all program listings, whether actual or on microfiche, will contain the following sections.

1. Storage Allocation
2. Program History
3. Documentation
4. Program Body
5. Symbolic Reference Table

Every page of a program listing contains a title line. On this line you will find:

- The name of the diagnostic
- The level of the compass assembler used
- Date and time of the assembly
- A page number

Page 1

Storage Allocation. This tells the beginning address of the program and how long it is.

Page 2 to End

The pages immediately following page 1 contain information as to revision levels and a history of corrections/enhancements made on the test.

Documentation usually follows next. This is the section of the listing containing the information previously found in the reference manual. The "*" located to the left of each line simply indicates the line as a comment. On the right side of each line is a name/number combination. This serves to uniquely identify each line

within the program. This information is used by update in the process of making changes to a program. Following the documentation, the program can be found. This is the section that contains the actual instructions to be executed by the machine.

Each line contains the following information, reading from left to right.

- Memory address in OCTAL - output from compass
- Instruction in OCTAL - output from compass
- Memory address symbol (optional) - input to compass
- Instruction mnemonic - input to compass
- Instruction data or address - input to compass
- Comments (optional) - input to compass
- Name/number - unique line identifier used by update

The last section of every program listing is called the Symbolic Reference Table. It is used to locate all symbols within the body of the program. Symbols are listed alphabetically top to bottom. Each line contains: The symbol, the address of the symbol, and a list of all references to the symbol, given as page/line. For example, 123/30 indicates a reference to the symbol occurred on page 123 of the listing, and on line 30 of that page.

POST TEST

When you have completed the learning activities assigned for module 11, sign on to the PLATO terminal and take the module 11 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 12.

MODULE 12

LABORATORY

STUDENT LAB MANUAL

TROUBLESHOOTING THE CPU

This module permits you hands-on experience in running and interpreting diagnostics and in troubleshooting instructor-induced CPU component failures.

DIRECTIONS

This module requires an instructor and laboratory equipment for all the learning activities. Approximately 32 hours should be allowed for the laboratory activities, none of which should last more than 6-8 hours at a time. Contact your course administrator to schedule your lab. You will work in a group of not more than three students. Read and observe the safety practices, and also read through the procedure portion of each learning activity prior to doing that activity.

Each learning activity contains a problem worksheet with instructor checkpoints. Have your instructor initial the checkpoints as you complete each problem. When you have completed all the problem worksheets for that learning activity, ask your instructor to initial the learning activity instructor checkpoint on the module title page.

Because this module uses a lab instructor to verify your activities there is no test on the objectives. Thus, you do not have to return to PLATO for the remainder of the course.

This module ends with an Instructor Confirmation page. When you have completed all the learning activities, ask your lab instructor to sign it. Then, remove this page from the student manual; fold and staple it as shown on the back of the page. Since the form is preaddressed and stamped, all you have to do is mail it. When the form is received by Engineering Services Education, an ESE administrator will award you mastery of this module by entering the information in your PLATO file.

R0404
PRA4932B

SAFETY PRACTICES

While working on computer system equipment, all engineers are expected to follow reasonable and appropriate precautions with respect to electrical, mechanical, and personal safety hazards. You should pay careful attention to all entries in the maintenance documentation labeled *DANGER* or *WARNING*, which identify hazardous areas or procedures encountered during system equipment maintenance. Follow these safety practices when working on equipment:

1. You are responsible for ensuring that no action on your part causes unsafe conditions that may expose customer personnel to hazards in any device.

2. You should never work alone on equipment having exposed operating mechanical parts or exposed hazardous power components. If you must do so, notify your EIC or manager. In any case, the following precautions must be observed:

   a. Someone familiar with the power-off controls must be in the immediate area.

   b. Personal jewelry (rings, wristwatches, bracelets, necklaces, and so forth) shall be removed. A small box in the CE tool kit makes a good storage place for these items.

   c. If using only one hand, keep the other free hand in your pocket.

   d. Avoid wearing loose articles of clothing that can be snagged and drawn into moving machinery. Roll sleeves above the elbow or wear short-sleeve shirts. Neckties, if required, should be tucked in between the second and third shirt button or fastened about 3 inches from the end with a tieback or tieclasp, preferably nonconductive. Do not use tiechains. Clip-on neckties are preferable. Regular neckties will pull free, if caught, without causing injury.

   e. Before starting equipment, ensure that no other CE or customer personnel are in a position where they could get hurt.

f. While working in equipment, put red tape strips across any power controls, or use do not operate tags where available.

3. Replace worn or broken tools or test equipment as quickly as possible.

4. If the machine is running, do not reach in to the works; remember, they are YOUR fingers.

5. If using a strobe light on mechanical devices, do not touch anything; what appears stationary could be moving.

6. Safety glasses or goggles must be used if you are:

   a. Driving pins, riveting, swaging, or performing similar activities.

   b. Using an electric drill, grinder, reamer, and so forth.

   c. Installing or removing springs under tension or compression.

   d. Using any type of solvent, spray, or chemical for cleaning or touch-up painting.

   e. Performing any other activity that could endanger the eyes. They are YOUR eyes, and you need them for this type of work.

7. When lifting, use a method that will not injure the spine or strain back muscles.

Above all, use good judgement and common sense - a moment of thought before you act can save hours of grief later.

ENGINEERING & SUPPORT
OPERATIONS
Last Revision: 12/82
Next Review: DEC '83

POLICY

ELECTROSTATIC
DISCHARGE
(ESD) PROTECTION

4.500

IN KEEPING WITH CORPORATE DIRECTION ON ELECTROSTATIC SENSITIVE COMPONENTS, THIS POLICY ESTABLISHES THE MINIMUM REQUIREMENTS AND PRACTICES WITHIN ENGINEERING SERVICES FOR HANDLING ALL ELECTRO-STATIC SENSITIVE COMPONENTS.

THE PURPOSE OF THIS POLICY IS TO MINIMIZE THE IMPACT OF ELECTROSTATIC DISCHARGE ON COMPONENTS, PRINTED WIRING BOARD ASSEMBLIES AND EQUIPMENTS, THEIR RELIABILITY, LIFE-CYCLE COSTS AND PROTECT THE INTEGRITY OF ESD CONTROLS IMPLEMENTED AT SUPPLYING DIVISIONS.

THE POLICY IS APPLICABLE TO THE HANDLING, SHIPPING, REPAIR AND STORING OF MICROCIRCUITS, PRINTED WIRING BOARD ASSEMBLIES, ASSEMBLIES, SUBASSEMBLIES AND EQUIPMENTS WITHIN THE SCOPE OF THE MANUFACTURING STANDARD 1.60.010 'HANDLING AND PACKAGING REQUIREMENTS FOR ELECTROSTATIC SENSITIVE DEVICES'.

ALL SEMICONDUCTORS, PRINTED WIRING BOARD ASSEMBLIES, AND SUBASSEMBLIES CONTAINING THESE COMPONENTS MUST BE HANDLED ONLY BY PROPERLY GROUNDED PERSONNEL. PACKAGING REQUIREMENTS WILL BE CONSISTENT WITH THE PRACTICES OF THE SUPPLYING DIVISIONS. IN MOST CASES THIS WILL REQUIRE THAT DEFECTIVE ITEMS BEING RETURNED FOR REPAIR BE PACKAGED IN THE ESD PROTECTIVE BAGS SUPPLIED WITH THE NEW PART AND GENERALLY BE SUBJECT TO STATIC SAFEGUARDING PROCEDURES DETAILED IN CDC MANUFACTURING STANDARD 1.60.010. ANY PACKAGING FOR THESE PARTS MUST TAKE PLACE AT A STATIC SAFEGUARDING WORKSTATION. REPAIR AND REWORK MUST BE ACCOMPLISHED ONLY AT STATIC SAFEGUARDED WORKSTATIONS PER REQUIREMENTS OF MANUFACTURING STANDARD 1.60.010.

ENGINEERING & SUPPORT
OPERATIONS
Last Revision: 12/82
Next Review: DEC '83

PROCEDURE

ELECTROSTATIC
DISCHARGE
(ESD) PROTECTION
CUSTOMER ENGINEER
HANDLING

4.501

THIS PROCEDURE APPLIES TO FIELD CUSTOMER ENGINEERS HANDLING ASSEMBLIES OR SUBASSEMBLIES CONTAINING SEMICONDUCTORS DURING EQUIPMENT REPAIR. THE ORDER OF STEPS IS ONLY FOR PURPOSE OF DOCUMENTING THE INFORMATION. IN THIS TEXT, THE WORD 'ASSEMBLY' IS USED TO INDICATE ASSEMBLY, SUBASSEMBLY, PART, MODULE, COMPONENT, PAK, ETC. (SEE ATTACHMENT A FOR EXCLUSIONS).

CUSTOMER ENGINEER

1. ASSEMBLIES MUST NOT BE REMOVED FROM THEIR STATIC SHIELDED BAG FOR GENERAL INSPECTION UNLESS IT IS DONE AT A STATIC SAFE WORKSTATION AND THE WRIST STRAP IS ON AND CONNECTED TO THE WORKSTATION.

2. ASSEMBLIES SHOULD ONLY BE HANDLED ON THE EDGES, CONTACT WITH THE CONNECTORS OR COMPONENTS SHOULD BE AVOIDED.

3. POWER SHOULD BE OFF THE EQUIPMENT WHEN REMOVING/INSTALLING ESD SENSITIVE ASSEMBLIES.

4. ASSEMBLIES MUST ONLY BE REMOVED FROM AN EQUIPMENT WHEN THE WRIST STRAP IS ON AND CONNECTED TO THE EQUIPMENT THE ASSEMBLY IS BEING REMOVED FROM.

5. ASSEMBLIES REMOVED FROM AN EQUIPMENT TO AFFECT A REPAIR MUST BE PLACED IN A STATIC SHIELDED BAG WHILE THE WRIST STRAP IS CONNECTED TO THE EQUIPMENT AND BEFORE THE ASSEMBLY IS LAID ASIDE.

6. A REPLACEMENT ASSEMBLY TO AFFECT A REPAIR MUST NOT BE REMOVED FROM THE STATIC SHIELDED BAG UNTIL THE WRIST STRAP IS ON AND CONNECTED TO THE EQUIPMENT UNDER REPAIR.

CUSTOMER ENGINEER

7. WHEN CHECKING AN ESD SENSITIVE ASSEMBLY IN AN EQUIPMENT WITH ANY TEST DEVICE, THE DEVICE LEADS SHOULD BE FIRST TOUCHED TO GROUND ON THE EQUIPMENT.

8. ASSEMBLIES RECEIVED BY THE FIELD IN STATIC SHIELDED BAGS MUST BE RETURNED TO WDC IN STATIC SHIELDED BAGS.

9. TEST THE WRIST STRAP MONTHLY USING AN OHMMETER.

   A. MEASURE FROM THE BANANA PLUG TO THE METAL STRIP ON THE INSIDE OF THE WRIST STRAP BAND.

   B. THE READING MUST BE BETWEEN 870K OHMS AND 1.5M OHMS.

   C. IF THE VALUE IN STEP 'B' IS NOT IN THE SPECIFIED RANGE, DISCARD THE WRIST STRAP AND OBTAIN A NEW ONE.

NOTE

THE WRIST STRAP CONTAINS A 1 MEG RESISTOR FOR CURRENT LIMITING AND USER SAFETY.

ENGINEERING & SUPPORT
OPERATIONS
Last Revision: 12/82
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PROCEDURE

ELECTROSTATIC
DISCHARGE
(ESD) PROTECTION
CUSTOMER ENGINEER
HANDLING

ATTACHMENT "A" 4.501

ALL SEMI-CONDUCTORS ARE SUSCEPTIBLE TO STATIC DISCHARGE IN VARYING DEGREES, THE LATER TECHNOLOGIES MORE SO THAN YEARS PAST. SOME OF THE OLD TECHNOLOGIES, 1604, 3000, 1700, 6000 AND 7000 FALL INTO THE GROUP OF LOW SUSCEPTIBILITY AND NEED NOT BE PROTECTED WITH STATIC SHIELDED BAG AND WRIST STRAP. ANY ASSEMBLY CONTAINING AN IC (INTEGRATED CIRCUIT) HOWEVER, SHOULD FOLLOW THE PROCEDURE AND BE PROTECTED REGARDLESS OF AGE OF TECHNOLOGY.

LEARNING ACTIVITIES

You must complete both of these learning activities. After completing each activity, ask your lab instructor to initial the instructor checkpoint.

Instructor Checkpoint	Activity	Description	Page
_____	12-A	Lab: Diagnostic Loading Laboratory: During this activity you learn how to load the CPU diagnostic.	
_____	12-B	Lab: SMM Diagnostic Usage Lab: During this activity you will load and learn about the various CPU Diagnostics, ET1, CT1, CT3, IMC, CU1, MAN ERX, and BD1/CMS.	
_____	12-C	Lab: Troubleshooting Lab. During this lab you will isolate problems induced into the CYBER 170 CPU by the instructor. ___a) Shift Network, Small arithmetic unit, RNI ___b) Boolean Sequence, Increment sequence, Normal Jump ___c) Shift Sequence, pack, unpack, normalize, FP Add/Subtract ___d) FP Multiply/Divide, FP End Case, Return Jump ___e) Exchange Jump, Error Exit ___f) Compare/Move	

INSTRUCTOR CONFIRMATION

INSTRUCTIONS: When all objectives in the preceding laboratory session have been met, complete this form. Please fill in all the information asked for in each blank space. Next, the form must be signed by the lab instructor in the space provided. Then, remove this page and fold it so that the address on the back appears. Then staple it and mail it. When this form is received by ESE, the student's PLATO records will be updated to reflect mastery of this lab module.

STUDENT NAME: _____
(print)

EMPLOYEE NUMBER: _____

DEPARTMENT NUMBER: _____

PLATO SIGN-ON NAME: _____
(print)

PLATO GROUP NUMBER_____

I certify that the above named student has satisfactorily completed all procedures and has met the objectives of Module 12 in the CYBER 170 Model 720/730 Central Processor course.

INSTRUCTOR NAME: _____
(print)

INSTRUCTOR SIGNATURE _____ DATE: _____

COURSE TITLE: CYBER 170 Model 720/730 Central Processor
PRODUCT NUMBER: R0404

INSTRUCTOR COMMENTS:

OBJECTIVES - Laboratory

L-1 Given the SMM Reference Manual, Pub. No. 60160600 and SMM Handouts, the student will interpret displays and error messages for EJ1 and CT1 CPU Diagnostics.

L-2 Given the SMM Tape or Disk and the SMM Reference Manual, Pub. No. 60160600, the student will run the following CPU diagnostics:

a. Run Diagnostics EJ1 and CT1

L-3 Given the SMM Tape or Disk and the SMM Reference Manual, Pub. No. 60160600, the student will locate a given CPU problem to within 3-5 packs using EJ1 and CT1 Diagnostics.

L-4 Given the SMM Reference Manual, Pub. No. 60160600 and SMM Handouts, the student will interpret displays and error messages for CT3 and IMC.

L-5 Given the SMM Tape or Disk and the SMM Reference Manual, Pub. No. 60160600, and SMM Handouts, the student will run the following CPU diagnostics:

a. Run Diagnostics CT1, CT3 and IMC

L-6 Given the SMM Tape or Disk and the SMM Reference Manual, Pub. No. 60160600, and SMM Handouts, the student will locate a given CPU problem to within 3-5 packs using CT1, CT3, and IMC.

L-7 Given the SMM Tape or Disk and the SMM Reference Manual, and SMM Handouts, the student will run the CPU following diagnostics:

a. Run Diagnostics CT1, CT3, ERX and MAN

L-8 Given the SMM Tape or Disk and the SMM Reference Manual, and SMM Handouts, the student will locate a given CPU problem to within 3-5 packs using CT1, CT3, ERX, and MAN.

L-9 Given the SMM Tape or Disk, SMM Reference Manual, and Student Handouts, the student will run the following CPU diagnostics:

a. Run Diagnostics BD1 and CMS

L-10 Given the SMM Tape or Disk, SMM Reference Manual, and SMM Handouts, the student will locate a given CPU problem to within 3-5 packs using CMS and BD1.

CYBER 172, 173, 174 CENTRAL PROCESSOR MAINTENANCE
STUDENT LAB MANUAL

INTRODUCTION

This manual will be used on lab days. It contains all directions to be followed. The labs are structured to include: SMM diagnostic usage and troubleshooting mainframe malfunctions.

Read the "Safety Practices" listed in this Manual.

Answer all questions and follow procedures as listed.

For each instructor induced malfunction, you must complete a problem worksheet. The main purpose of this worksheet is to monitor your progress on troubleshooting. Be sure the instructor checks your sheet (Instructor checkpoint) before swapping any modules.

After locating the malfunction, complete the comments section and discuss your progress with the instructor.

It is our intent that by doing this you will develop your own technique to problem solving. Work as accurately and as quickly as you can. Your work in the lab will be evaluated on the following criteria:

1. Logical approach - i.e., running appropriate diagnostics, entering your own programs, operands, etc.

2. Location of failing logic module.

3. The time it takes for you to find the malfunction.

The troubleshooting procedures are set up to include problems from the previous day's theory plus problems that relate to any of the material covered up to that point in the course.

STUDENT LAB MANUAL

DAY: 1

SUBJECT: Shift Network, Small Arithmetic, RNI and Initial Start, Using EJ1 and CT1.

OBJECTIVES:

L-1 Given the SMM Reference Manual and SMM Handouts, the student will interrupt displays and error messages for EJ1 and CT1 Diagnostics.

L-2 Given the SMM Tape or Disk and the SMM Reference Manual, the student will run the following CPU diagnostics:

a. Run Diagnostics EJ1 and CT1

L-3 Given the SMM Tape or Disk and the SMM Reference Manual, the student will locate a given CPU problem to within 3 to 5 packs using EJ1 and CT1 Diagnostics.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts, and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or 720/730 System

PROCEDURE:

1. Deadstart Machine from Disk

2. Set 2X Speed Call: MTR
   Command: SR2X
   1-D Drop Monitor

3. Load Diagnostic EJ1
   Command: EJ1

4. Set Stop at End of Section
   Command:

5. Set Stop at End of Test
   Command:

6. Start the Diagnostic
   Command:

7. When it Stops at the End of the Section Clear Stop at End of Section Parameter
   Command:

8. Start Again
   Command:

9. While the Diagnostic is Running Bring Up the Exchange Package Displays
   Command:

10. The Next Time it Stops Should be the End of the Test. Clear the Stop at End of Test Parameter
    Command:

11. Start Test Again
    Command:

12. This is the Way the Test Normally Runs

13. Have the Instructor Install a Demonstration Bug

14. The Remaining Time will be Spent Troubleshooting Bugs. Have the Instructor install a Bug. Fill out a Problem Worksheet for each Bug. When completed have the Instructor initial the Worksheets.

PROBLEM WORKSHEET

DAY 1 BUG NUMBER One

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 1 BUG NUMBER Two

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

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PROBLEM WORKSHEET

DAY 1 BUG NUMBER Three

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 1 BUG NUMBER Four

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

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PROBLEM WORKSHEET

DAY 1 BUG NUMBER Five

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 1 BUG NUMBER Six

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 1 BUG NUMBER Seven

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 1 BUG NUMBER Eight

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

STUDENT LAB MANUAL

DAY: 2

SUBJECT: Boolean Sequence, Increment Sequence and Normal Jump Sequence using CT1 and BJ1

OBJECTIVES:

L-1 Given the SMM Reference Manual and SMM Handouts, the student will interrupt displays and error messages for EJ1 and CT1 CPU Diagnostics.

L-2 Given the SMM Tape or Disk and the SMM Reference Manual, the student will run the following CPU diagnostics:

a. Run Diagnostics EJ1 and CT1

L-3 Given the SMM Tape or Disk and the SMM Reference Manual, the student will locate a given CPU problem to within 3 to 5 packs using EJ1 and CT1 Diagnostics.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts, and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or 720/730 System

PROCEDURE:

1. Deadstart Machine from Disk

2. Go to 2X Speed
   Command:

3. Load Diagnostic CT1
   Command:

4. Start the Test
   Command:

5. When it Stops it will be at the End of the Quicklook Section - Start Part 2 of the Command Test
   Command:

6. When it Stops at the End of the Test set Stop at End of Section Parameter
   Command:

7. Start the Test and note the Displays as it runs a Section at a time. Space to Start after every section
   Command:

8. Have the Instructor install a Demonstration Bug.

9. The remaining time will be spent Troubleshooting Bugs. Have the Instructor install a Bug. Fill out a Problem Worksheet for each Bug. When Sheet is completed have the Instructor initial it.

PROBLEM WORKSHEET

DAY 2 BUG NUMBER One

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Two

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Three

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Four

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

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PROBLEM WORKSHEET

DAY 2 BUG NUMBER Five

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Six

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Seven

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Eight

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

DAY: 2

SUBJECT: Shift Sequence, Pack and Unpack and Normalize Network using CT1, CT3 and IMC

OBJECTIVES:

L-3 Given the SMM Tape or Disk and the SMM Reference Manual, the student will locate a given CPU problem to within 3 to 5 packs using EJ1 and CT1 Diagnostics.

L-4 Given the SMM Reference Manual and SMM Handouts, the student will interrupt displays and error messages for CT3 and IMC .

L-5 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will run the following CPU diagnostics:

a. Run Diagnostics CT1, CT3 and IMC

L-6 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will locate a given CPU problem to within 3 to 5 packs using CT1, CT3 and IMC.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts, and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or 720/730 System

PROCEDURE:

1. Deadstart the Machine from Disk

2. Load SMM system
   Command:

3.

4. Load Diagnostic CT3
   Command:

5. Start the Test
   Command:

6. Observe the Running Displays

7. The remaining time will be spent Troubleshooting Bugs. Have the Instructor install a Bug. Fill out a Problem Worksheet for each Bug. When Sheet is completed have the Instructor initial it.

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Nine

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Ten

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Eleven

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Twelve

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Thirteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Fourteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

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PROBLEM WORKSHEET

DAY 2 BUG NUMBER Fifteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Sixteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

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DAY: 2 and 3

SUBJECT: Floating Point Add and Subtract, Floating Multiply and Divide, Floating Point End Case and Return Jump Sequence Using CT1, CT3 and IMC

OBJECTIVES:

L-6 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will locate a given problem to within 3 to 5 packs uing CT1, CT3 and IMC.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts, and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or 720/730 System

PROCEDURE:

1. Deadstart the Machine from Disk

2. Load SMM system
   Command:

3.

4. Load Diagnostic IMC
   Command:

5. Start the Test
   Command:

6. Observe the Running Displays

7. The remaining time will be spent Troubleshooting Bugs. Have the Instructor install a Bug. Fill out a Problem Worksheet for each Bug. When the Sheet is completed have the Instructor initial it.

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Seventeen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Eighteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 2 BUG NUMBER Nineteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER One

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Two

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Three

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Four

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Five

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

DAY: 3

SUBJECT: Error Exit, Exchange Jump Sequence and ECS Instructions Using CT1, CT3, ERX and MAN

OBJECTIVES:

L-6 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will locate a given CPU problem to within 3 to 5 packs using CT1, CT3 and IMC.

L-7 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will run the following CPU diagnostics:

a. Run Diagnostics CT1, CT3, ERX and MAN

L-8 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will locate a given CPU problem to within 3 to 5 packs using CT1, CT3 and ERX and MAN.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or 720/730 System

PROCEDURE:

1. Deadstart the Machine from Disk

2. Load SMM system
   Command:

3. Load the Diagnostic MAN
   Command:

4. Start the Test
   Command:

5. When the test stops change parameters so sec 10 is not run
   Command:

6. Start the test

7. Deadstart and go to 2X Speed
   Command:
   NOTE: CEJ/MEJ Switch must be off (Disabled)

8. Load the Diagnostic ERX
   Command:

9. Start the Diagnostic
   Command:

10. What is checked by the different sections of the test?
    Section 1 -
    Section 2 -
    Section 3 -
    Section 4 -

11. Deadstart from disk
    Command:

12. Load SMM system

13. Load the command buffer XP400
    Command:

14. Enter the following programs using the conditions stated and execute them. After execution fill in the blanks and note the conditions that caused these results.

1. CONDITIONS: CEJ/MEJ Disabled
EM = 7
P = 000020
(000020) = 44123 46000 46000 46000
X2 = 2000 0000 0000 0000 0006
X3 = 2000 0000 0000 0000 0002

Run the program and note the contents of the following:

X1 =

(RA) =

P =

2. CONDITIONS: CEJ/MEJ Disabled
EM = 7
P = 000010
(000010) = 46000 30123 46000 46000
X2 = 3777 7000 0000 0000 0000
X3 = 2000 0000 0000 0000 0006

Run the program and note the contents of the following:

X1 =

(RA) =

P =

3. CONDITIONS: CEJ/MEJ Disabled
EM = 7
P = 000030
(000030) = 10122 36312 14433 72543
X2 = 0000 0000 0000 1111 1111

Run the program and note the contents of the following:

X1 =

X3 =

X4 =

X5 =

(RA) =

P =

4. CONDITIONS: CEJ/MEJ Disabled
EM = 1
P = 000020
FL = 001000
(000020) = 10100 51100 02000 43225
X0 = 2525 2525 2525 2525 2525
(002000) = 7777 7777 7777 7777 7777

Run the program and note the contents of the following:

X1 =

X2 =

A1 =

(RA) =

P =

5. CONDITIONS: CEJ/MEJ Disabled
EM = 5
P = 000040
FL = 002000
(000040) = 10600 51600 02000 10766
X0 = 2525 2525 2525 2525 2525
X7 = 0000 0000 0000 0000 7777

Run the program and note the contents of the following:

X6 =

X7 =

A1 =

(002000) =

(RA) =

P =

6. CONDITIONS: CEJ/MEJ Disabled
EM = 7
P = 000010
(000010) = 14211 00000 40312 46000
X1 = 3777 0000 0000 0000 0002

Run the program and note the contents of the following:

X2 =

X3 =

(RA) =

P =

The remaining time will be spent Troubleshooting Bugs. Have the Instructor install a Bug. Fill out a Problem Worksheet for each Bug. When the sheet is completed have the Instructor initial it.

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Six

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

R0404
PRA4932B

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Seven

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Eight

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Nine

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Ten

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

R0404
PRA4932B

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Eleven

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Twelve

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 3 BUG NUMBER Thirteen

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

DAY: 4

SUBJECT: Compare/Move Incrementor using BD1 and CMS Diagnostics

OBJECTIVES:

L-9 Given the SMM Tape or Disk and the SMM Reference Manual and SMM Handouts, the student will run the following CPU diagnostics:

a. Run Diagnostics BDI and CMS

L-10 Given the SMM Tape or Disk, SMM Reference Manual and SMM Handouts, the student will locate a given CPU problem to within 3 to 5 packs using CMS and BD1.

REFERENCES: CYBER 170 Models 720/730 Central Processor Unit Diagrams, Pub. No. 60456170
SMM Handouts, and CPU References
SMM Reference Manual, Volume 1 and 2, publication number 60160600

EQUIPMENT/TOOLS: CYBER 173 or CYBER 720/730 System

PROCEDURE:

1. Deadstart the Machine from Disk

2. Load SMM system

3. Load the Diagnostic BD1 into PPU6

4. Start the test command: Space bar

5. What is being checked by the different sections of the test?

   Section 0 - Move Direct
   Section 1 - Move Indirect
   Section 2 - Compare Uncollated
   Section 3 - Compare Collated
   Section 4 - AOR
   Section 5 - Exchange Jumps and Memory Conflicts

6. When the test finishes change the parameters to loop on to the compare collated section without stopping commands:

8. Load the Diagnostic CMS command:

9. Start the Diagnostic and Observe the Running Displays command:

10. The remaining time will be spent troubleshooting bugs. Have the instructor install a bug. Fill out a problem worksheet for each bug. When the sheet is completed have the instructor initial it.

PROBLEM WORKSHEET

DAY 4 BUG NUMBER One

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 4 BUG NUMBER Two

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

R0404
PRA4932B

PROBLEM WORKSHEET

DAY 4 BUG NUMBER Three

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 4 BUG NUMBER Four

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

R0404
PRA4932B

PROBLEM WORKSHEET

DAY 4 BUG NUMBER Five

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

PROBLEM WORKSHEET

DAY 4 BUG NUMBER Six

FAILING DIAGNOSTICS:

SIGNIFICANT ERROR DISPLAYS:

LIST SUSPECTED FAILING LOGIC:

INSTRUCTOR CHECKPOINT _____

BAD MODULE:

COMMENTS:

TIME ON: _____
TIME OFF: _____
INSTRUCTOR INITIALS: _____

R0404
PRA4932B

APPENDIX A
USING INDIVIDUALIZED INSTRUCTION

If this is your first experience with individualized instruction, you probably have a few questions. The information that follows will help you understand the nature of individualized instruction.

WHAT IS INDIVIDUALIZED INSTRUCTION?

Individualized instruction is a teaching method that is oriented toward the individual rather than the group. Individualized instruction--

- Determines what skills you possess that pertain to the topic of instruction.
- Determines what skills you must acquire.
- Allows you to acquire these skills at your own pace by studying a variety of learning activities.

Individualized instruction is structured around a student manual that guides you through the course and is also a learning resource. The student manual is divided into modules.

Each module contains information that will help you meet the objectives of that module. The information within the module is presented in learning activities.

MAY I WORK WITH OTHER STUDENTS?

Yes, if two or more of you are taking the course at the same time, it may be beneficial for you to do some of the learning activities together. Whether you work alone or with others depends on your needs.

HOW DO I PROCEED THROUGH THE COURSE?

You begin the course by signing on to the PLATO terminal. See appendix B for detailed instructions for signing on. You may want to take the pretest or you may ask for a full assignment that teaches all of the objectives of the first module. If you take the pretest, PLATO learning management (PLM) will evaluate the results of the test and assign the learning activities that are keyed to the objectives you did not master. Then, study the

assigned learning activities and retake the test. If you are successful, proceed to the next module and repeat the process until course completion. If not, study the assigned learning activities and retake the test until you master all the module objectives.

See figure A-1 for a flowchart illustrating your progress through the course.

HOW DO MODULES, COURSES, AND CURRICULA RELATE TO EACH OTHER?

The structure of the Engineering Services Training Program has three parts (see figure A-2):

- Module. A module is made up of learning activities. It contains objectives and test questions. A module teaches specific training tasks. For example, a module could cover electrical/mechanical adjustments.

- Course. A course is made up of modules. A course covers a single subject, for example, a course on the oscilloscope or magnetic tape unit.

- Curriculum. A curriculum is made up of courses. It covers a broad area of knowledge, for example, an entire subsystem. A curriculum may contain courses that range in complexity from introductory to advanced.

WHAT KIND OF RESOURCES ARE USED IN INDIVIDUALIZED INSTRUCTION?

Individualized learning activities use the following resources and combinations of those resources to present information.

- Text Reading. This resource presents information via the student manual and provides simplified explanations, drawings, and examples.

- Reference Reading. This resource directs you to read designated pages in a specified reference manual.

- Exercises. This resource presents information via the student manual. It uses a question/answer presentation. An exercise may be used to present new material or it may determine your comprehension of previously presented material.

- Programmed Text. This resource is a student manual text reading that presents information and asks for immediate feedback to determine your comprehension.

- Laboratory. This resource gives you actual hands-on experience with computer equipment.

- PLATO Assisted Learning. This resource presents information via the PLATO terminal.

Appendix A

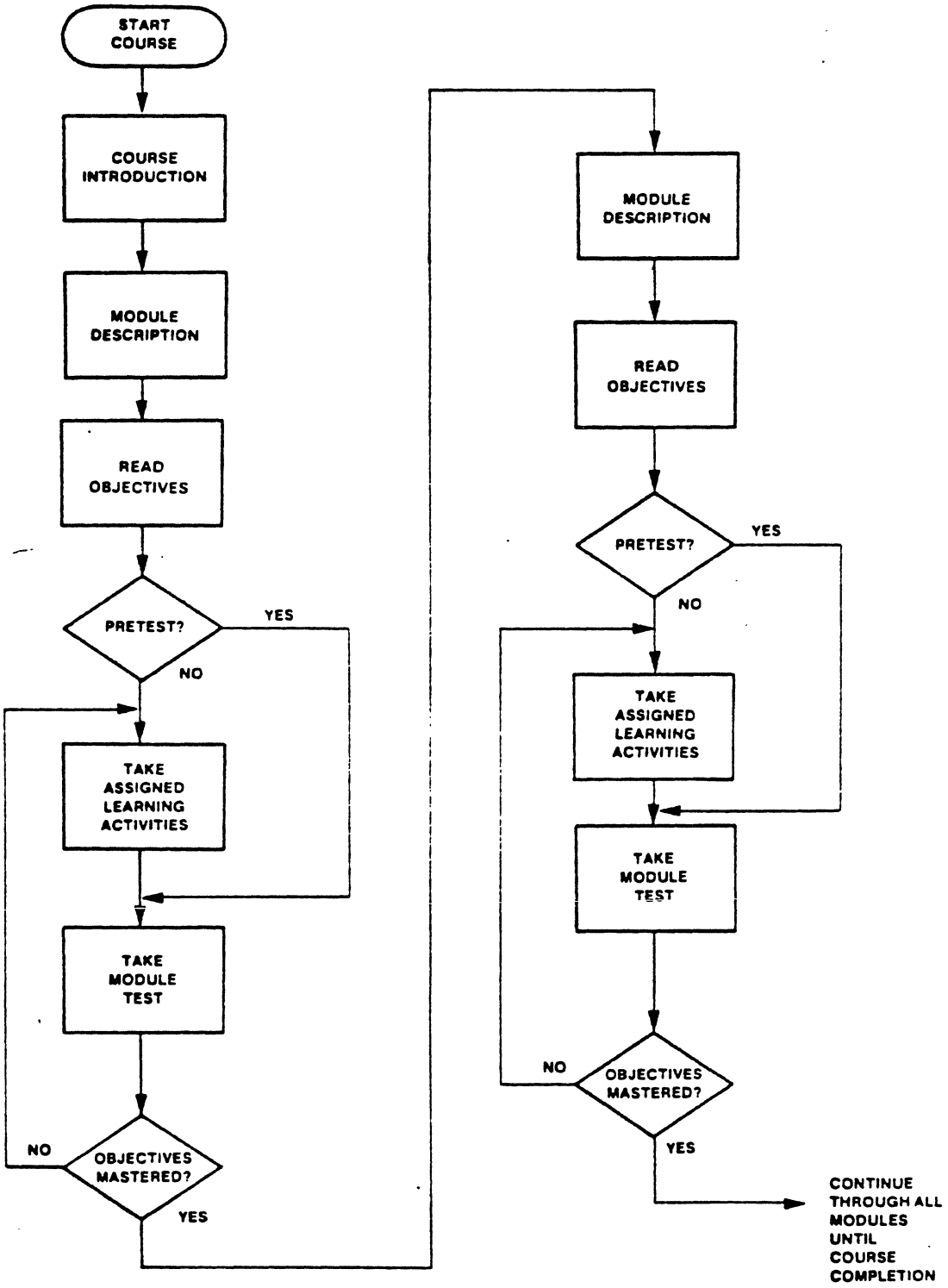

Figure A-1. Student Progress

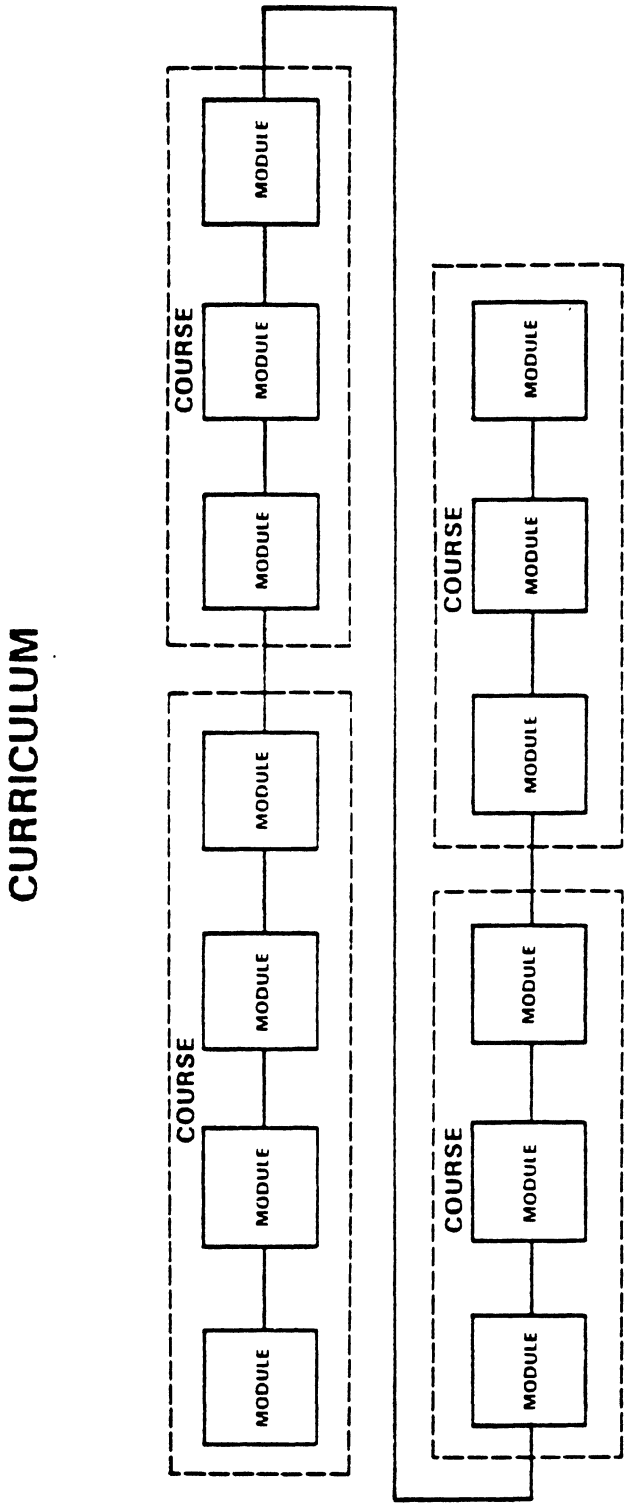

Figure A-2. Program Structure

- Audiotape. This resource presents an audio message via an audiotape machine.
- Microfiche. This resource uses a microfiche viewer and microfiche film to illustrate information.
- Videotape. This resource uses a videotape playback unit and videotape to present information.

You may proceed from one learning activity to another at your own pace. The learning activites are not long, but it is important that you take the time to understand the material before you go on to the next activity.

Each learning activity is coded with a number and a letter. The number stands for the module and the letter represents the order in which the learning activity is presented. The first learning activity of the first module is Learning Activity 1-A. The second activity is 1-B, and so on.

HOW DO I TAKE A TEST?

All testing is managed by PLATO learning management (PLM). PLM performs three important functions:

- Administers all tests.
- Assigns learning activities based on the results of the tests.
- Retains your student records for all courses you take within a curriculum.

PLM has two modes of testing, on-line and off-line. On-line testing requires that you sign on to a PLATO terminal to take the test. When you complete the test, PLM will assign learning activities based on the results of your test.

On-line testing is preferred because it saves time and enables you to proceed through your training without any delays.

Off-line testing is the more traditional method. Your administrator will give you a copy of the test and an answer sheet. Do not write on the test; record all your answers on the answer sheet. Return your test to the administrator, who will grade it and enter the results into the PLM system.

WHAT IS THE INDIVIDUALIZED INSTRUCTION TESTING PHILOSOPHY?

A test is a device that determines whether you have met the objectives of the course (module). It determines if you have acquired the skills that the course is designed to teach.

The number of times you take a test or your score on the test is not as important as the information you gain from the test results. The results tell you what areas you need to study.

Do not be alarmed if you need to take a test more than once. It is not your scores that count, it is your ability to perform your job that is important to you, Engineering Services' customers, and Control Data.

WHO ARE THE PERSONNEL INVOLVED IN INDIVIDUALIZED INSTRUCTION?

Regional Education Manager (REM)

The REM manages the training program for the region/country. He coordinates and administrates training activities to ensure that training needs are identified and fulfilled.

Regional Training Coordinator (RTC)

The RTC works with the education center manager to provide assistance as required; for example, he orders training materials, processes enrollments/confirmations, etc.

Education Center Manager (ECM)

The ECM administrates and coordinates training activities to ensure training delivery. For example, he provides a technical training advisor and identifies training materials requirements for the RTC. This individual may be a resource center manager, regional education manager, skill center manager or education center manager.

Education Training Coordinator (ETC)

The ETC manages the PLATO learning management (PLM) system. He provides the student with a student sign-on and PLM entries, and he works with the education center manager to solve PLM related problems.

Technical Advisor (TA)

The TA deals directly with the student. He monitors activities and provides guidance and assistance as required. A TA may be an engineer-in-charge, regional technical support instructor or a customer engineer with technical expertise.

Subject Matter Expert (SME)

The SME provides technical assistance for training problems that cannot be resolved by the technical advisor.

Learning Center Administrator (LCA)

The LCA works directly with the student to ensure smooth progression through the course.

APPENDIX B
PLATO SIGN-ON PROCEDURES

In order to begin the course you must first sign on to the PLATO system. Depending on where your terminal is located, you may first have to dial up the PLATO computer in order to establish communication between the computer and your terminal. If your terminal is on a direct connection, this is not necessary, and steps 2 and 3 can be skipped.

1. Turn power on.

*2. Dial the number of the PLATO system using the data phone. When the system answers, you will hear a tone. The next step must be performed within three seconds after you hear the tone.

*3. Lift exclusion button (usually located on the telephone cradle). Place the receiver on the table or in front of the cradle. Do not hang up.

NOTE

Some data phones require that you lift the exclusion button to dial, and hang up when the tone is heard.

4. Press the STOP key on the PLATO terminal keyboard.

5. Press the NEXT key on the PLATO keyboard. This causes the welcome to PLATO page to be displayed (figure B-1).

6. Enter your name exactly as you are registered in this course. Normally this will be your last name, followed by a space, and your first initial, with no capital letters (for example, smith j, as shown in figure B-2).

   If you make a mistake, you can erase it by pressing the ERASE key on the right side of the keyboard.

7. Press the NEXT key. You will then be asked to enter the name of your PLATO group . Enter the name of the PLATO group in which you are registered. Once again, the exact spelling is required.

---

*Dial-up system only.

Appendix B

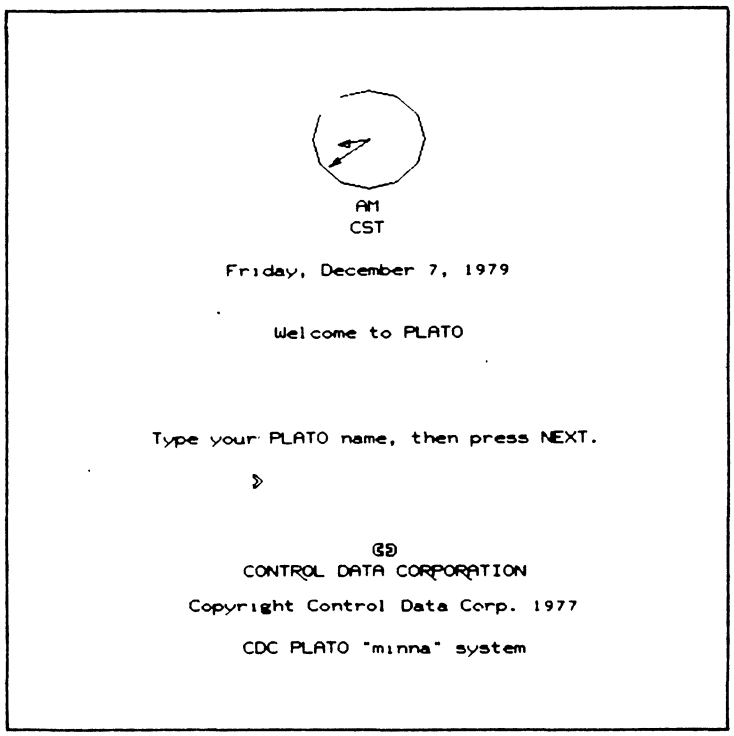

Figure B-1. Welcome to PLATO

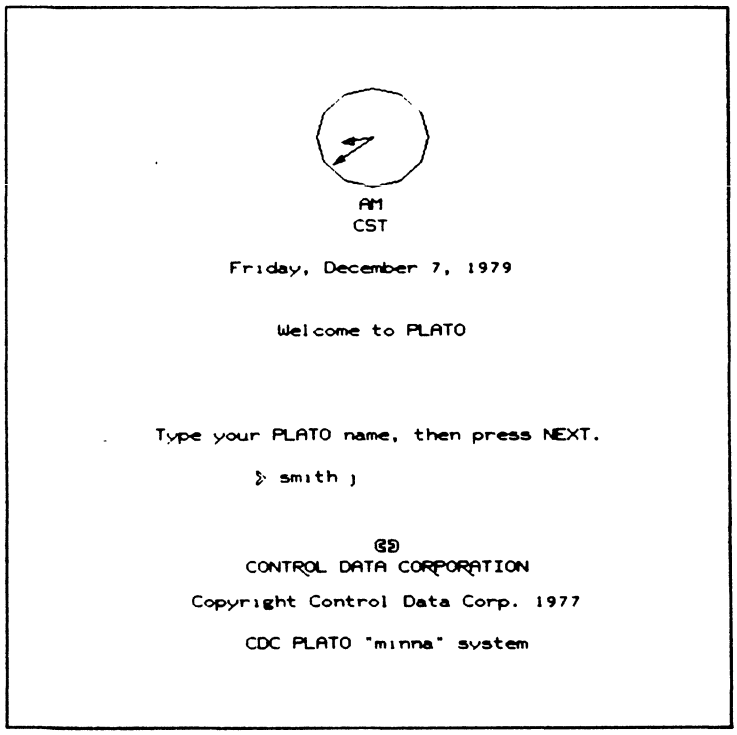

Figure B-2. Repeat

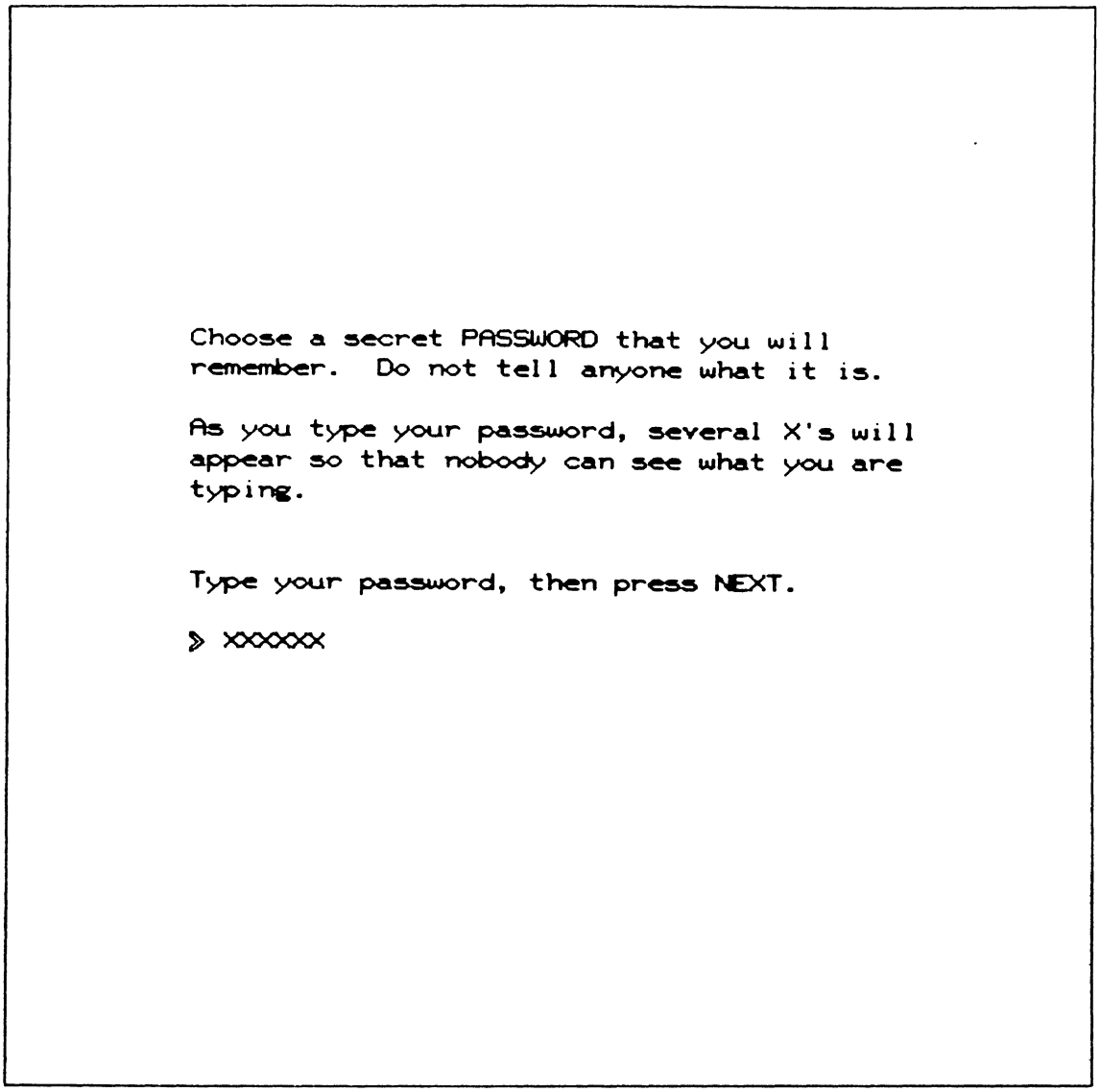

Figure B-3. Password

8. Hold down the SHIFT key and press the STOP key. You will then be asked to enter your password (figure B-3). Your password can be anything you choose, but it must be something that you can easily remember, such as a name, phone number, employee number, etc. Do not forget the password you have selected. It will become your key for gaining access to your lessons.

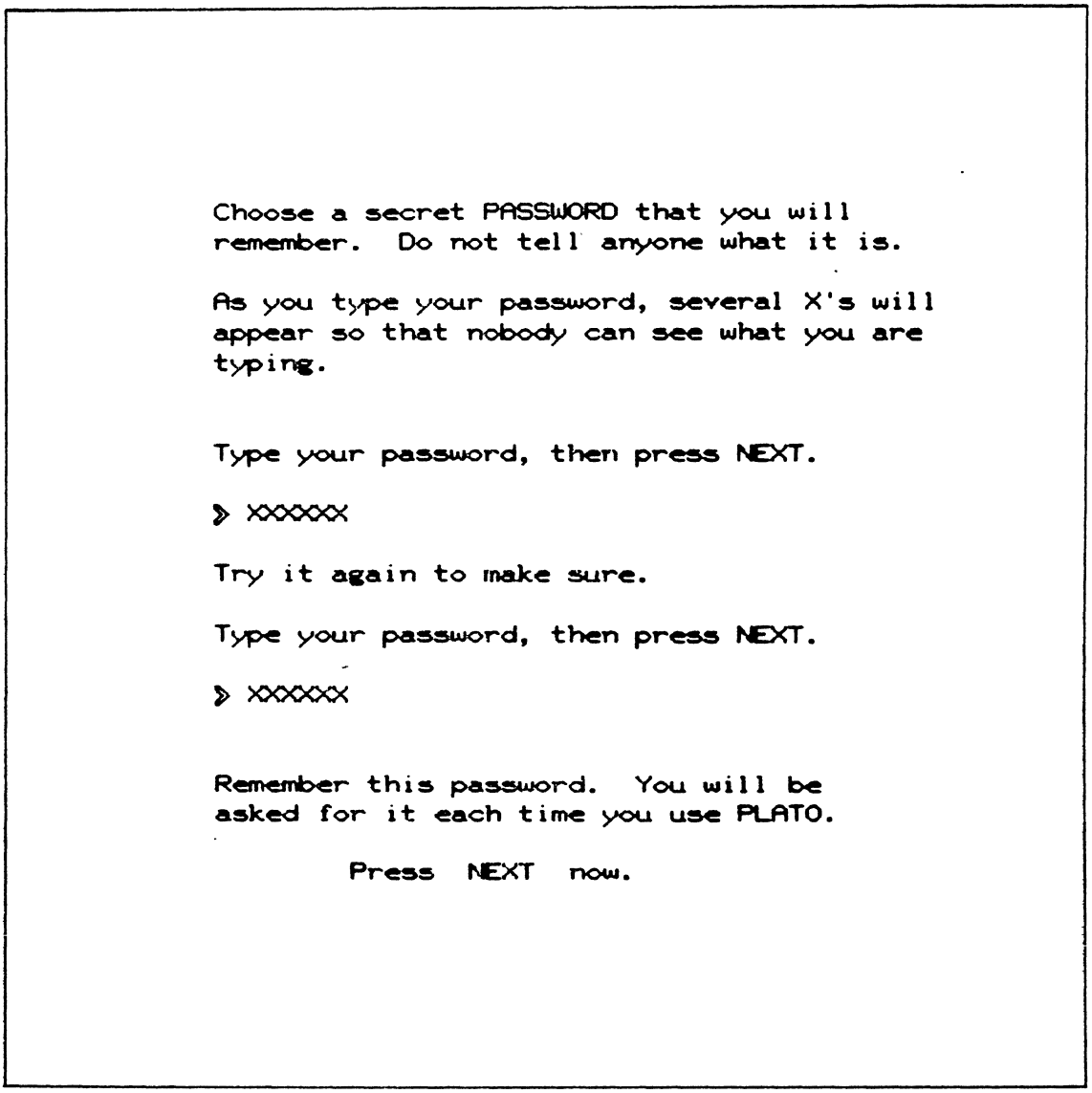

Figure B-4. Password Repeat

9. Press the NEXT key. If this is the first time you have signed on to this course, you will be asked to enter your password again (figure B-4). Enter it again, just as you did before. From this point on you will be required to enter your password only once when you sign on.

10. Press NEXT. You are now signed on to the system.

APPENDIX C
USING MICROFICHE

INTRODUCTION

This appendix provides the basics of selecting, loading, and viewing microfiche on a Micron 780 Microfiche Desk Reader or a similar reader. (See the Microfiche Handbook, available from Information Services, STP109, for more information.)

The portable microfiche desk reader may also be used since it has the same capabilities as the Micron 780.

Consult the operator's manual for specific information on the readers.

SELECTION

Select the proper microfiche by consulting the microfiche header, which contains the title of the contents and the microfiche reference number (figure C-1).

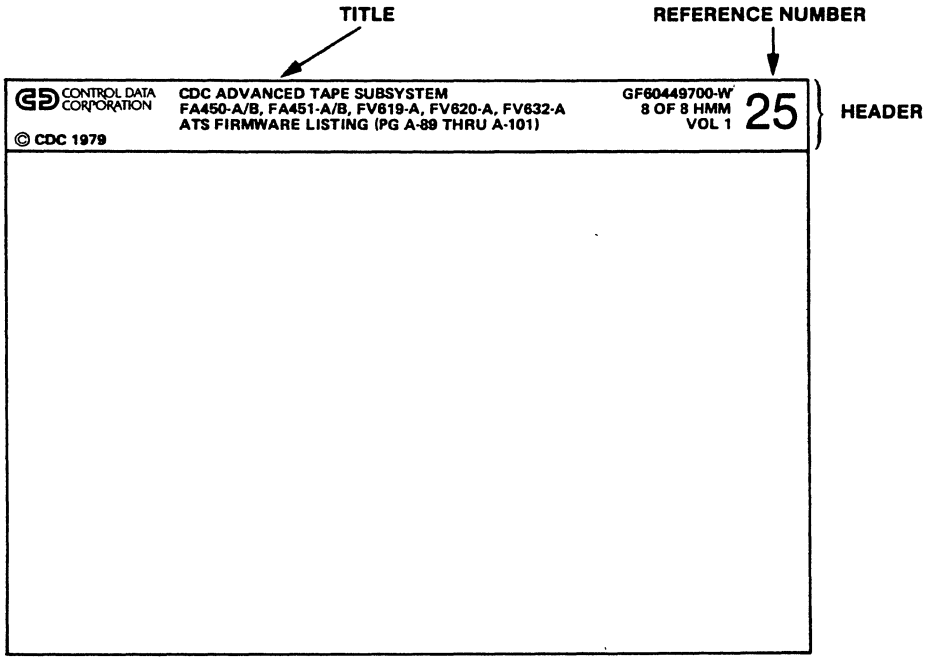

Figure C-1. Microfiche

(Manual Title)
Appendix C

LOADING

To load the Micron 780 Desk Reader or a similar desk reader, perform the following procedure (figure C-2).

1. Turn on the microfiche desk reader by pushing in on the side of the LOW-OFF-HIGH switch that indicates a low light intensity setting.

2. Pull the carriage assembly toward you until the glass covers flip up.

3. Hold the microfiche by the header with the printed information facing up (figure C-3).

4. Position the microfiche toward the upper right corner of either glass.

5. Push the carriage assembly back and position it so that a full picture with a index grid coordinate number is visible on the screen.

6. Select the proper index grid. Each microfiche desk reader is equipped with two index grids, a 24X index grid for 24X microfiche and a 42X index grid for 42X microfiche; most documentation is on 24X microfiche (figure C-4).

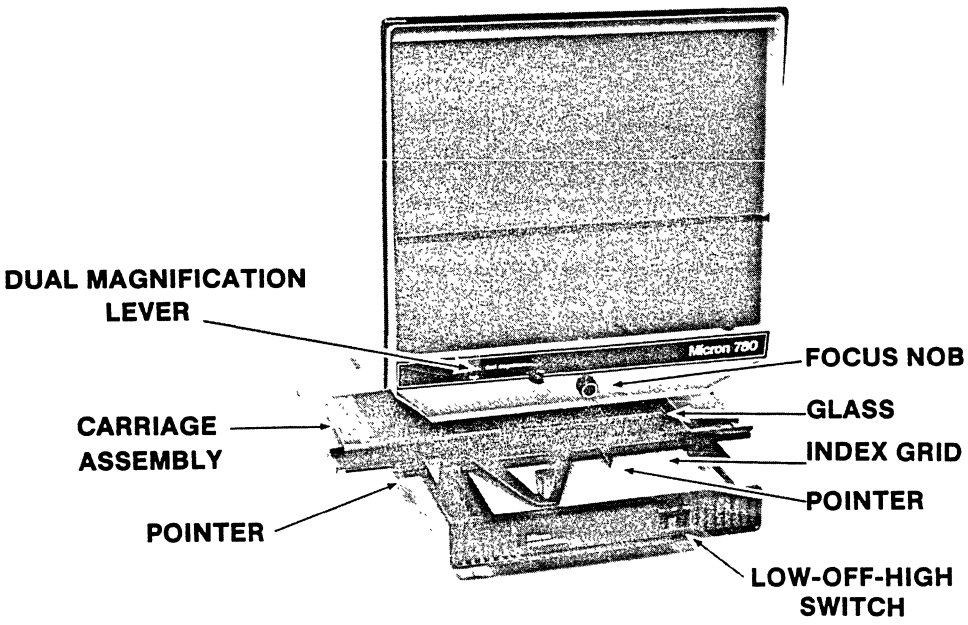

Figure C-2. Microfiche Desk Reader

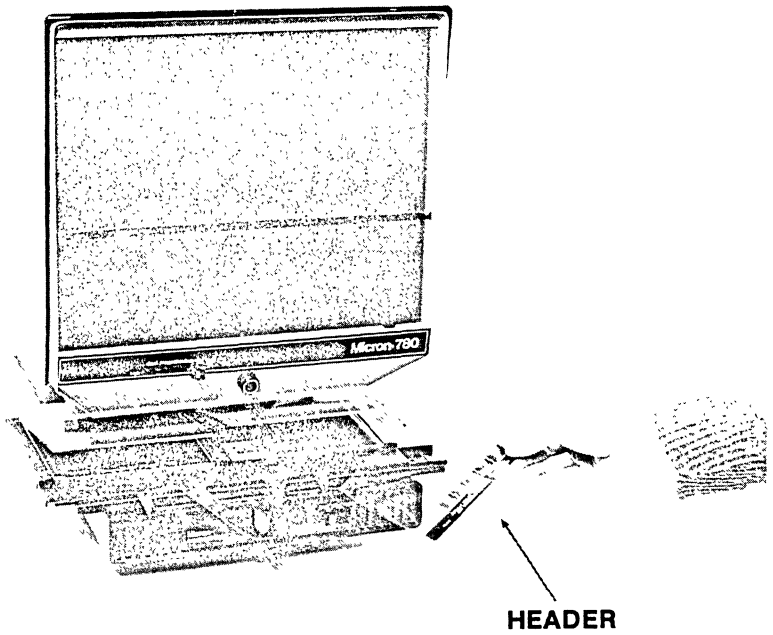

Figure C-3. Inserting Microfiche into Desk Reader

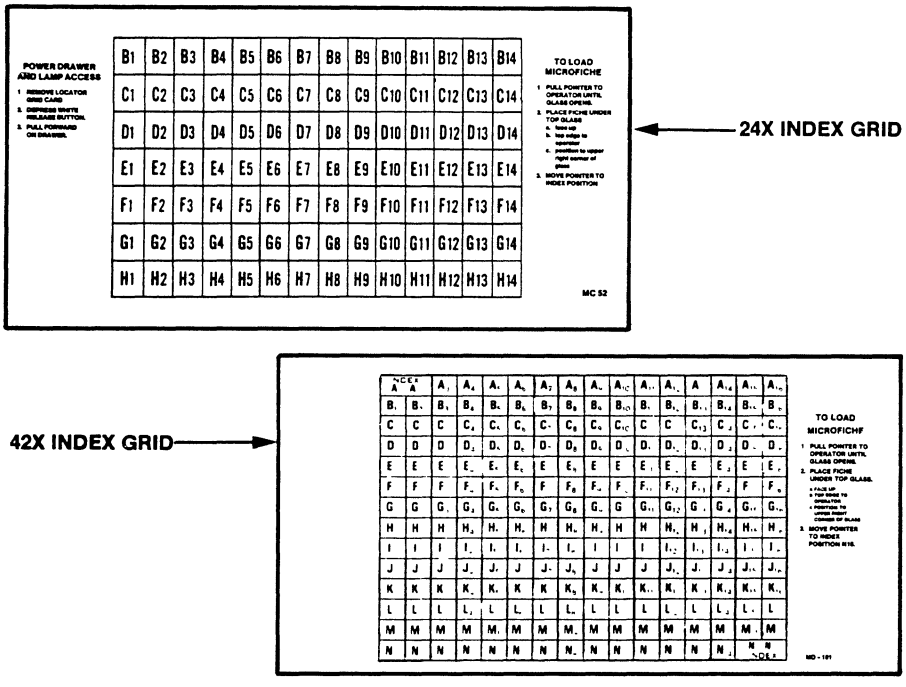

Figure C-4. 24X and 42X Index Grids

a. The 24X microfiche has a 3/8-inch header, and the 24X index grid is divided into 14 horizontal boxes.
b. The 42X microfiche has a 1/2-inch header, and the 42X index grid is divided into 16 horizontal boxes.

7. Place the proper index grid so that the carriage pointer is centered over the index grid coordinate number that appears on the screen.

VIEWING

When viewing a logic diagram with a index grid coordinate number of B1, position the carriage pointer between B1 and B2 on the index grid. Adjust the carriage to obtain a full screen picture. Student manuals and audiotapes may call the coordinates B1/B2 on the index grid. B1/B2 indicates that the carriage pointer should be positioned between B1 and B2 on the index grid (figure C-5).

Other pages of technical manual can be viewed by placing the carriage pointer in the center of the index grid coordinate number (figure C-6).

Screen Quadrants

The desk reader screen is divided into four quadrants to reference any area of the screen (figure C-7). It has a transparent horizontal yellow line for the horizontal axis; you may need to add the vertical axis. Transparent map tape, clear tape, or grease pencil work well as the vertical axis.

Magnification

A dual lense microfiche reader, such as the Micron 780, can magnify any area of a 24X microfiche by using the high (42X) lense in the following procedure.

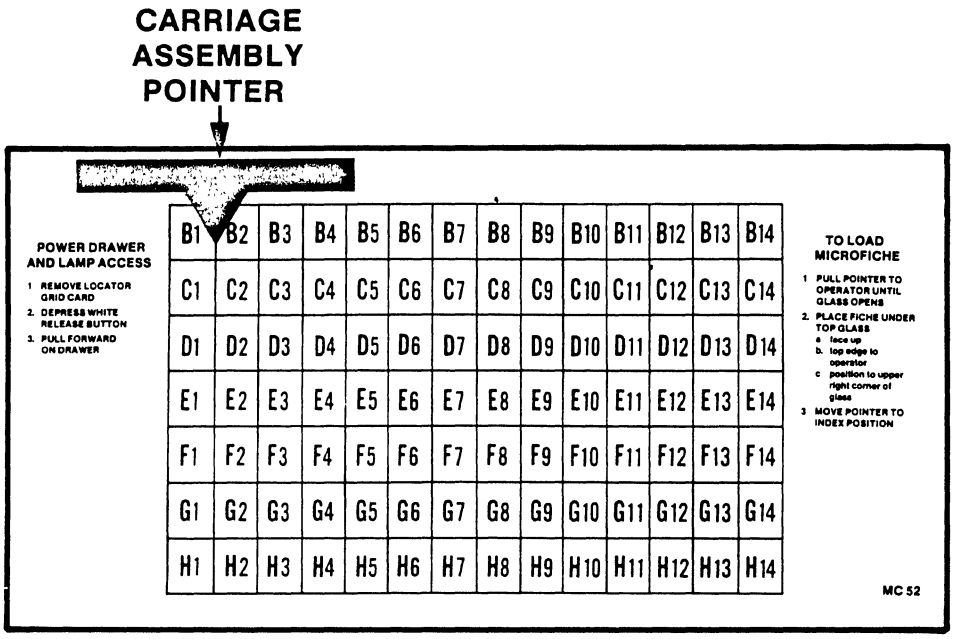

Figure C-5. Carriage Assembly Pointer Position for Technical Manuals

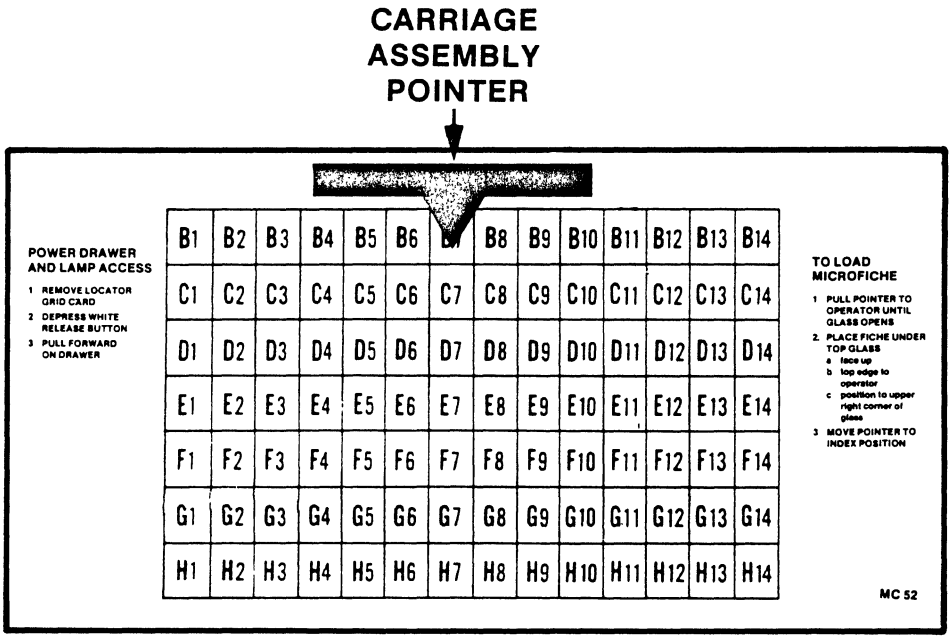

Figure C-6. Carriage Assembly Pointer Position for Logic Diagrams

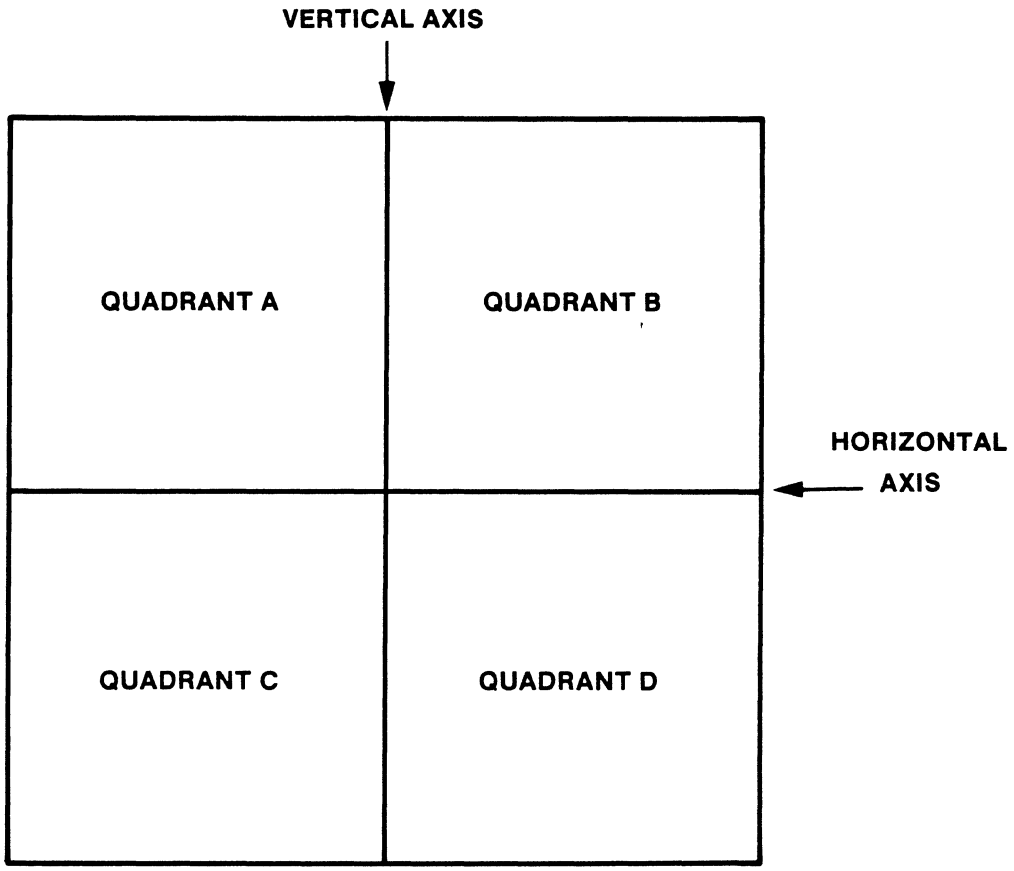

Figure C-7. Screen Quandrants

1. Position the area that you wish to magnify in the center of the screen using the carriage assembly (see figure C-2 for the location of the DUAL MAGNIFICATION lever).

2. Move the DUAL MAGNIFICATION lever to HIGH.

3. Return the magnification lever to LOW before moving on to another frame.

Light Intensity

The microfiche desk reader can deliver high or low light intensity. The Light Intensity switch is part of the LOW-OFF-HIGH switch.

The following suggestions may help reduce eye strain when using a microfiche desk reader for a long time.

- Do not watch the screen while moving to a different frame.
- Use low intensity light for low magnification and high intensity light for high magnification.
- Be sure the image on the screen is focused sharply (see figure C-2 for the location of the focus nob).
- Tilt the projector forward or backward.
- Vary the intensity of the room lighting.

Be sure to turn the viewer off whenever you are not using it. Extended exposure to light will fade the microfiche.

COMMENT SHEET

MANUAL TITLE CYBER 170 MODEL 720/730 CENTRAL PROCESSOR VOLUME 2

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